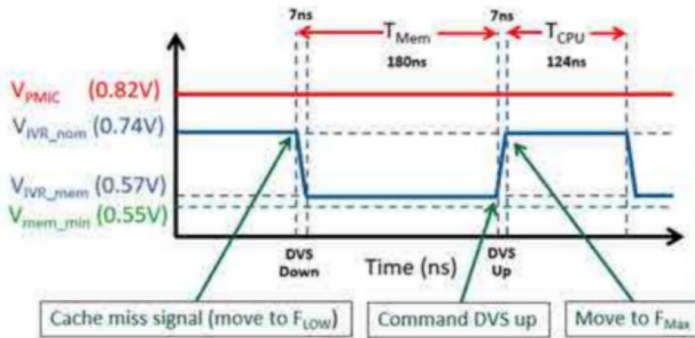


SPECIAL REPORT : POWER SUPPLIES + MAGNETICS

*Utilize Ultra-Fast DVS saves energy during cache misses ($P \propto F * V^2$)*



Model Example Assumptions:

- CPU F_{max} = 1.6 GHz, 1.0 clock cycle per instruction
- CPU F_{min} = 0.567 / 0.742 * 1.6 GHz = 1.22 GHz
- Cache miss rate = 0.5%
- Memory access time = 180ns (includes DVS down)
- Empower DVS up & down time of 7ns

Metric	VR Type	Operating Segment			SoC Total per Cycle
		Mem Wait Cycle	DVFS (Up & Down)	CPU Cycle	
Time (ns)	RIVR	173	7+7	124	311
	PMIC	180	0	124	304
Avg Voltage (V)	RIVR	0.57	0.65	0.74	0.64
	PMIC	0.82	0.82	0.82	0.82
Current (A)	RIVR	4.50	5.20	7.71	6.0
	PMIC	8.5	8.5	8.5	8.5
Avg Power (W)	RIVR	2.55	3.40	5.72	3.9
	PMIC	7.0	7.0	7.0	7.0
Energy (uJ)	RIVR	0.44	0.05	0.71	1.20
	PMIC	1.26	0	0.87	2.13

65% savings during wait cycle

Figure 4: DVS can improve efficiency in memory fetch operations

voltage scaling (DVS).

DVS is a power management technique that in real-time optimizes the supply voltage to minimize losses based on supplying the lowest possible voltage for operation at a given time. With DVS that is up to 1000 times faster than conventional designs, new generations of IVRs enable fast and lossless processor power state changes in nanoseconds. Nearly instantaneous voltage delivery eliminates excess voltage and, thus, wasted power. The result is dramatically improved efficiencies when controlling CPUs, GPUs and any other fast, clock-driven digital silicon. This is because nearly all of these components use power states (frequency-voltage combinations) that seek to minimize power-per-operation. Fast DVS not only removes wasted power on-state transitions, but also allows the system to forego the vagaries of having to predict future operat-

ing commands in determining the correct power state.

A good example of how ultra-fast DVS impacts efficiency can be seen by considering memory fetch operations.

A modern-day CPU typically has multiple levels of on-chip cache memory. This is used for maintaining high-speed performance by keeping what is likely to be the data needed for upcoming operations on-chip. Even with this significant amount of local memory, the CPU still misses the information it needs to perform a task around 0.5% of the time or about once every 200 fetches. This is known as a 'cache miss'.

If a cache miss occurs, the CPU has to request data from an off-chip memory location, typically forcing it to wait 180 ns or more for that data to arrive. With that tight of a window, trying to save

power by dropping the supply voltage with a traditional PMIC would be futile – DVS times there are measured in μ s. But with an IVR DVS time of say 10ns, it becomes possible to quickly drop the voltage to save power and raise it quickly back when the data arrives.

Efficiency Through Integration

In addition to improved transient response and DVS, the IVR's high level of integration in a small form factor also contribute to better overall system efficiency.

The tiny die size and integration capability of the IVR enable it to be coupled very closely to the digital load. The IVR die solution footprint is small enough to be mounted directly onto a substrate within the SoC itself. Furthermore, the die thickness can be as little as 100um to enable mounting on the bottom side of a substrate to fit within the height of a BGA.

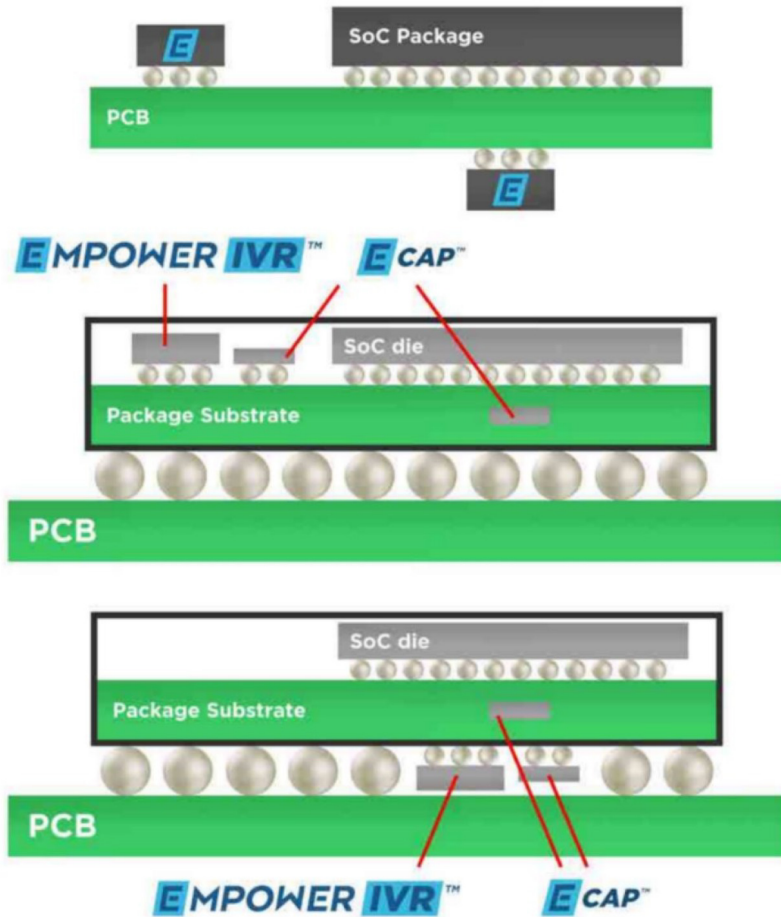


Figure 5: Tiny, integrated IVRs can be closely coupled to the load

By integrating the IVR in a die solution the close coupling of the load not only eliminates the I^2R losses, but it also eliminates the need for large banks of decoupling capacitors. This capability increases the system efficiency while further reducing the number of components and overall system cost.

The overall system savings is dramatic when considering the significant reduction in board

space while capitalizing on the performance benefits. Efficiency can be maximized while features such as DVS and the incredible load transient can enable system

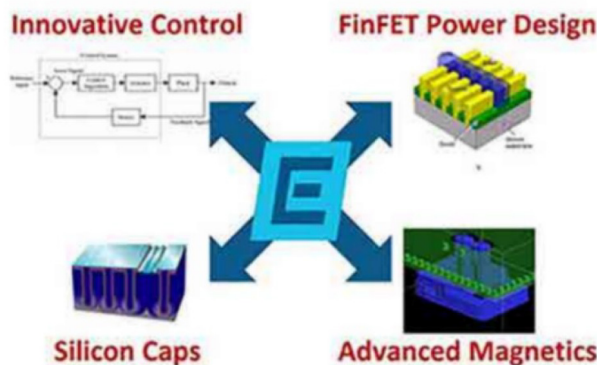


Figure 6: High levels of integration brings together FET, control circuits, passives and magnetics in a single IC

performance features not possible before.

Next-Generation IVRs

Empower's EP70XX family of step-down converters illustrates the latest generation of high-performance integrated voltage regulators. Built on an advanced CMOS geometry platform and using patented digitally configurable technology, devices in this high-frequency family can operate directly from a 1.8 V input supply or as the second stage of a two-stage conversion topology. The ICs are available with single-, dual- or triple- regulated outputs and integrate all of the discrete components needed for a complete power supply into a single, compact chip-scale BGA package with dimensions of just 5 mm x 5 mm. This makes them up to ten times smaller than more conventional voltage regulation circuits built around discrete semiconductors and passive components.

Empower
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