Regulation Efficiency for Data-Intensive Applications

Transient response, dynamic voltage scaling and integration are the keys to minimizing power losses

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It is estimated that by 2025 the annual size of real-time data in the global 'datasphere' will have increased tenfold from the level in 2018, reaching a total of 51 zettabytes. Indeed, driven in part by the pandemic, global internet traffic grew by around 35% in 2020 as a result of rapid uptake of video streaming, video conferencing, online gaming, and social networking.

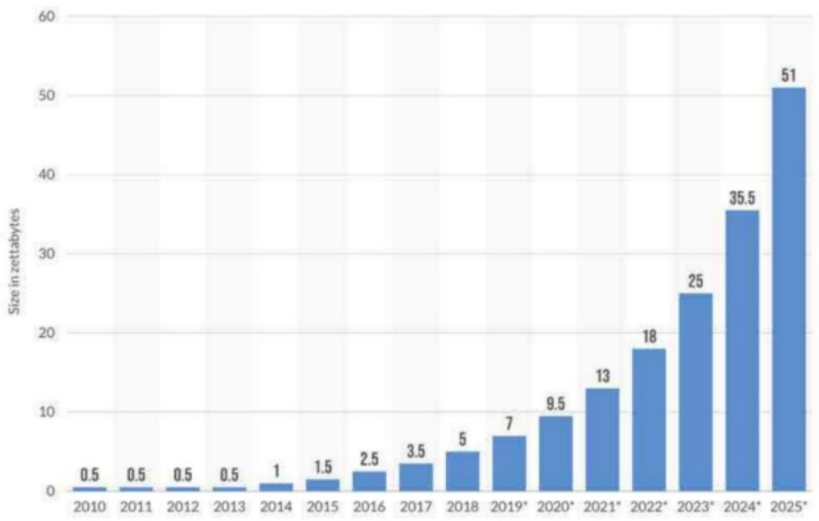


Figure 1: Real-time data in the global 'datasphere' will reach 51 zettabytes by 2025

Supporting these levels of data demands increasingly powerful semiconductor technologies. These include next-generation processors such as Intel's 'Sky Lake' and 'Ice Lake' or AMD's 'Rome' platforms with potential power requirements of between 300 W and 450 W. Some of the latest GPUs demand powers as high as 600 W, while FPGAs and a whole host of acceleration technologies add further to the power overhead.

For engineers, the challenge is meeting both the power needs of these processor technologies and system efficiency targets that result not only from commercial pressure to keep energy costs down but from environmental targets that mandate better use of energy. Addressing this challenge is leading to a re-imagining of the power management ICs (PMICs) within the power delivery network in terms of transient response, dynamic voltage scaling (DVS) and end-to-end integration.

Integrated Voltage Regulators

According to Transparency Market Research, the total global market for all PMICs is predicted to reach $56.48 billion in 2026. Much of this demand is led by voltage regulators. These are essential components for preventing operational disruption through the maintenance of one or more voltages at pre-defined levels and the regulation of power delivery to processor ICs and other power-hungry devices and circuits.

The need to provide, amongst other functions, input and output filtering, circuit protection, programmability and feedback loops means that conventional voltage regulator PMICs have to be combined with external, discrete components such as bulky capacitors, resistors and inductors. Now, however, there is an alternative to this approach in the form of the integrated voltage regulator (IVR).

IVRs are high-performance switching voltage regulators that monolithically integrate the voltage regulator semiconductor and all of the necessary discrete components into a single device. Such integration simplifies the design and implementation of voltage regulation circuitry, improves efficiency by eliminating connection losses, reduces susceptibility to EMI, minimizes the bill of materials, enhances overall reliability and reduces PCB footprint.

Among the ways that that IVRs deliver improved efficiency when compared to conventional PMICs is in terms of their response to transients.

Transient Response and Efficiency

Maintaining a steady voltage when there are significant changes in load current is critical to voltage regulation. The transient response of the chosen regulator to such load current changes is, therefore, key to successful operation. As system performances improve and processor speeds continue to rise, many existing PMICs are becoming too slow to react to changing loads and to return to steady-state voltage after a transient. When the processor being powered suddenly increases the supply current requirement, for example by jumping in frequency, the power supply will dip while the output current ramps up to match. The steady-state voltage must then be increased to account for this dip. Because power is proportional to voltage squared, the more the steady-state voltage has to be increased to account for this, the more steady-state energy is wasted.

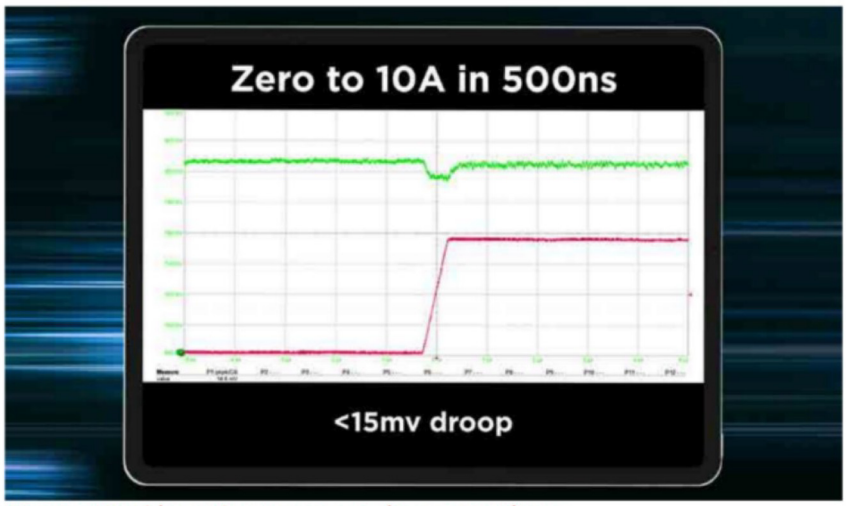


Figure 2: Rapid transient response reduces power losses

By combining high levels of integration with proprietary control techniques, the latest IVRs can deliver tight voltage regulation through ultra-fast transients and offer settling times that are up to one hundred times shorter than those of traditional regulators. This is because traditional converters must operate at low frequencies (0.3 MHz to 3 MHZ) to achieve high efficiency, necessitating several large capacitors for output and input filtering if they are to achieve reasonable transient response. Being able to ramp the output current so much faster allows an IVR's output voltage dip to reduce by one third or less with recovery times one hundred times faster than today's best-in-class DC/DC converters.

Efficiency and Dynamic Voltage Scaling

Another important contribution to system efficiency derives from how the regulator handles dynamic

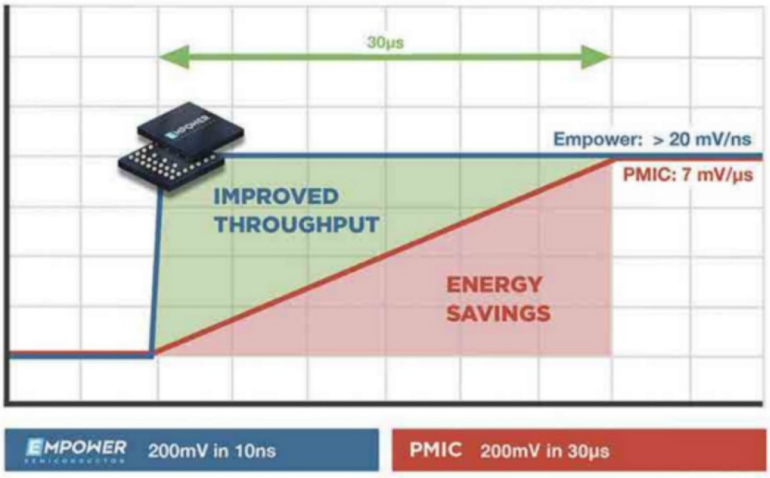
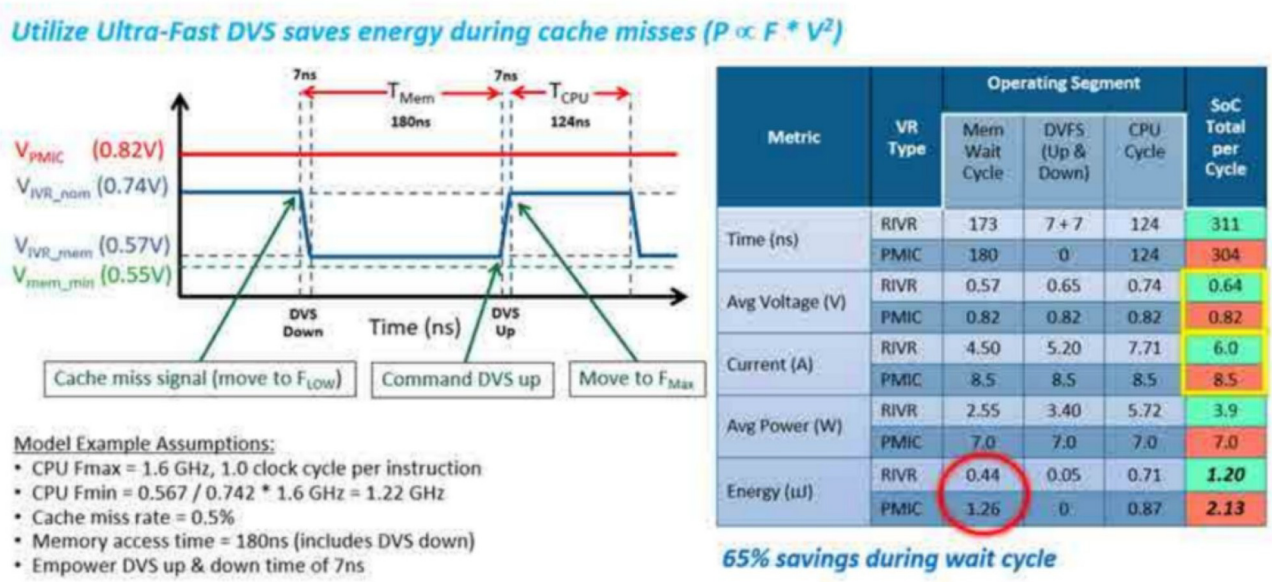


Figure 3: DVS of Empower IVR versus conventional PMIC



Metric	VR Type	Operating Segment			SoC Total per Cycle
		Mem Wait Cycle	DVFS (Up & Down)	CPU Cycle	
Time (ns)	RIVR	173	7+7	124	311
	PMIC	180	0	124	304
Avg Voltage (V)	RIVR	0.57	0.65	0.74	0.64
	PMIC	0.82	0.82	0.82	0.82
Current (A)	RIVR	4.50	5.20	7.71	6.0
	PMIC	8.5	8.5	8.5	8.5
Avg Power (W)	RIVR	2.55	3.40	5.72	3.9
	PMIC	7.0	7.0	7.0	7.0
Energy (uJ)	RIVR	0.44	0.05	0.71	***1.20***
	PMIC	1.26	0	0.87	***2.13***

Figure 4: DVS can improve efficiency in memory fetch operations

voltage scaling (DVS).

DVS is a power management technique that in real-time optimizes the supply voltage to minimize losses based on supplying the lowest possible voltage for operation at a given time. With DVS that is up to 1000 times faster than conventional designs, new generations of IVRs enable fast and lossless processor power state changes in nanoseconds. Nearly instantaneous voltage delivery eliminates excess voltage and, thus, wasted power. The result is dramatically improved efficiencies when controlling CPUs, GPUs and any other fast, clock-driven digital silicon. This is because nearly all of these components use power states (frequency-voltage combinations) that seek to minimize power-per-operation. Fast DVS not only removes wasted power on-state transitions, but also allows the system to forego the vagaries of having to predict future operating commands in determining the correct power state.

A good example of how ultra-fast DVS impacts efficiency can be seen by considering memory fetch operations.

A modern-day CPU typically has multiple levels of on-chip cache memory. This is used for maintaining high-speed performance by keeping what is likely to be the data needed for upcoming operations on-chip. Even with this significant amount of local memory, the CPU still misses the information it needs to perform a task around 0.5% of the time or about once every 200 fetches. This is known as a 'cache miss'.

If a cache miss occurs, the CPU has to request data from an off-chip memory location, typically forcing it to wait 180 ns or more for that data to arrive. With that tight of a window, trying to save power by dropping the supply voltage with a traditional PMIC would be futile – DVS times there are measured in µs. But with an IVR DVS time of say 10ns, it becomes possible to quickly drop the voltage to save power and raise it quickly back when the data arrives.

Efficiency Through Integration

In addition to improved transient response and DVS, the IVR's high level of integration in a small form factor also contribute to better overall system efficiency.

The tiny die size and integration capability of the IVR enable it to be coupled very closely to the digital load. The IVR die solution footprint is small enough to be mounted directly onto a substrate within the SoC itself. Furthermore, the die thickness can be as little as 100um to enable mounting on the bottom side of a substrate to fit within the height of a BGA.

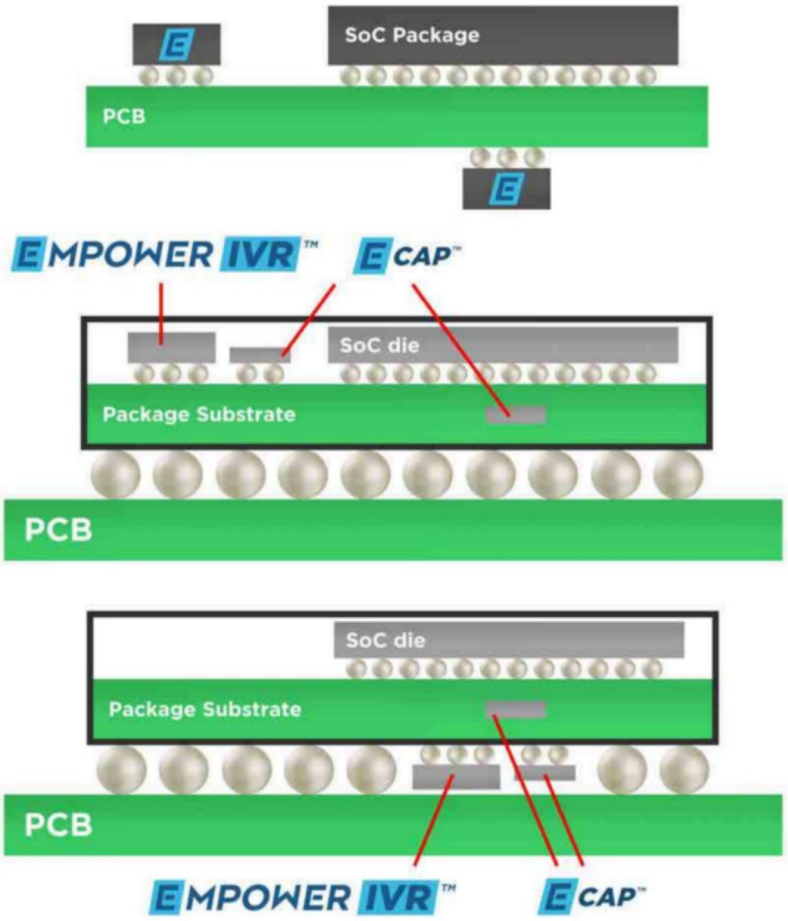


Figure 5: Tiny, integrated IVRs can be closely coupled to the load

By integrating the IVR in a die solution the close coupling of the load not only eliminates the I2R losses, but it also eliminates the need for large banks of decoupling capacitors. This capability increases the system efficiency while further reducing the number of components and overall system cost.

The overall system savings is dramatic when considering the significant reduction in board space while capitalizing on the performance benefits. Efficiency can be maximized while features such as DVS and the incredible load transient can enable system performance features not possible before.

Next-Generation IVRs

Empower's EP70XX family of step-down converters illustrates the latest generation of high-performance integrated voltage regulators. Built on an advanced CMOS geometry platform and using patented digitally configurable technology, devices in this high-frequency family can operate directly from a 1.8 V input supply or as the second stage of a two-stage conversion topology. The ICs are available with single-, dual- or triple- regulated outputs and integrate all of the discrete components needed for a complete power supply into a single, compact chip-scale BGA package with dimensions of just 5 mm x 5 mm. This makes them up to ten times smaller than more conventional voltage regulation circuits built around discrete semiconductors and passive components.

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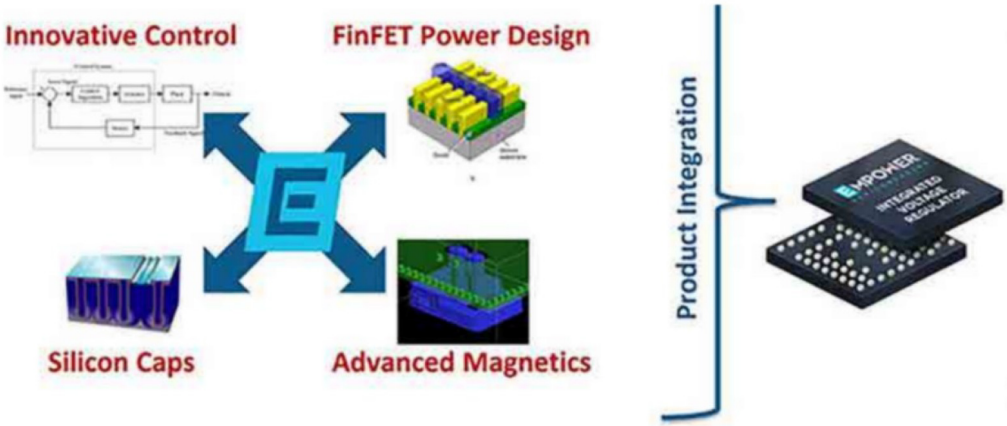

Figure 6: High levels of integration brings together FET, control circuits, passives and magnetics in a single IC