EP6070 *Single Output 28V / 15A Synchronous Buck Regulator*

Features

- Wide input voltage range: 6.5V to 28V
- 15 A continuous output current
- Output voltage adjustable down to 0.6V (±1.0%)
- Low $RDS_{(ON)}$ internal NFETs
  - 11 mΩ high-side
  - 4.5 mΩ low-side
- Constant On-Time with input feed-forward
- Programmable on-time up to 3.5 µs
- Selectable PFM light-load operation
- Ceramic capacitor stable
- Adjustable soft start
- Ripple reduction
- Power Good output
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Over voltage protection
- Thermal shutdown
- Thermally enhanced 4 mm x 4 mm QFN-23L package

Applications

- Portable computers
- Compact desktop PCs
- Servers
- Graphics cards
- Set-top boxes
- LCD TVs
- Cable modems
- Point-of-load DC/DC converters
- Telecom/Networking/Datacom equipment

Description

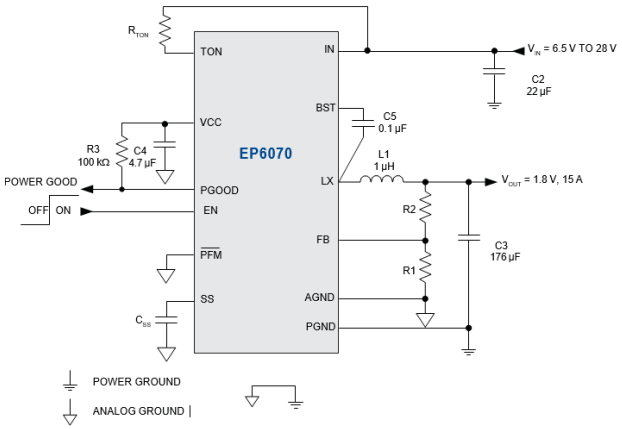
The EP6070 is a high-efficiency, easy-to-use DC/DC synchronous buck regulator that operates up to 28V. The device is capable of supplying 15A of continuous output current with an output voltage adjustable down to 0.6V (±1%).

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range. The on-time can be externally programmed up to 3.5µS.

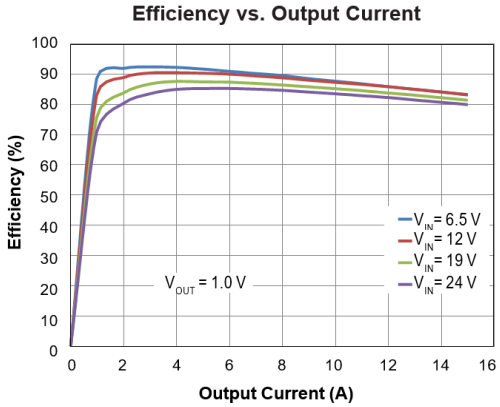
The device features multiple protection functions such as V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The EP6070 is available in a 4 mm × 4 mm QFN- 23L package and is rated over a -40°C to +85°C ambient temperature range.

Typical Application



Efficiency Chart



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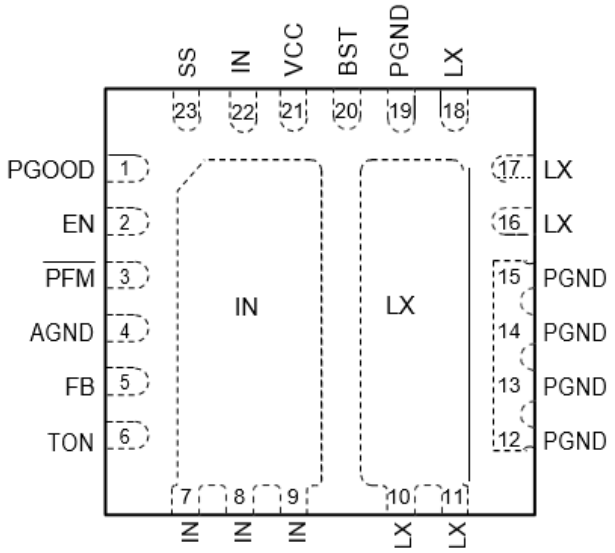
2 Ordering Information

Part Number	Description	Package	Carrier
EP6070	Single Output 15A DC-DC Converter	23-Pin 4 mm x 4 mm QFN	Tape and Reel



23-Pin 4 mm x 4 mm QFN (Top View)

2.1 Pin Descriptions

Pin Name	Pin No.	Description
1	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage for or 20% higher than the nominal regulation voltage. PGOOD is pulled lowduring soft-start and shut down.
2	EN	Enable Input. The EP6070 is enabled when EN is pulled high. The device shuts down whenEN is pulled low.
3	$\overline{\text{PFM}}$	PFM Selection Input. Connect PFM pin to VCC for forced PWM operation. Connect PFM pin toground for PFM operation to improve light load efficiency.
4	AGND	Analog Ground.
5	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator'soutput and AGND.
6	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on time.
7, 8, 9, 22	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
12, 13, 14, 15, 19	PGND	Power Ground.

10, 11, 16, 17, 18	LX	Switching Node.
20	BST	Bootstrap Capacitor Connection. The EP6070 includes an internal bootstrap diode. Connectan external capacitor between BST and LX as shown in the typical application.
21	VCC	Supply Input for analog functions. Bypass VCC to AGND with a 4.7µF~10µF ceramic capacitor.Place the capacitor close to VCC pin.
23	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.

3 Specifications

3.1 Absolute Maximum Ratings

Parameter	Rating
IN, TON to AGND	-0.3V to 30V
LX to AGND(1)	-1V to 30V
BST to AGND	-0.3V to 36V
SS, PGOOD, FB, EN, VCC, PFM to $\overline{\text{AGND}}$	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(2)	2kV

3.2 Recommended Operating Conditions

Parameter	Rating
Supply Voltage (V_{IN})	6.5V to 28V
Output Voltage Range	0.6V to 0.85*V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Operating Junction Temperature (T_J)	-40°C to +145°C
Package Thermal Resistance **(θ_{JA})** **(θ_{JC})**	 32°C/W 4°C/W
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(2)	2kV

Notes:

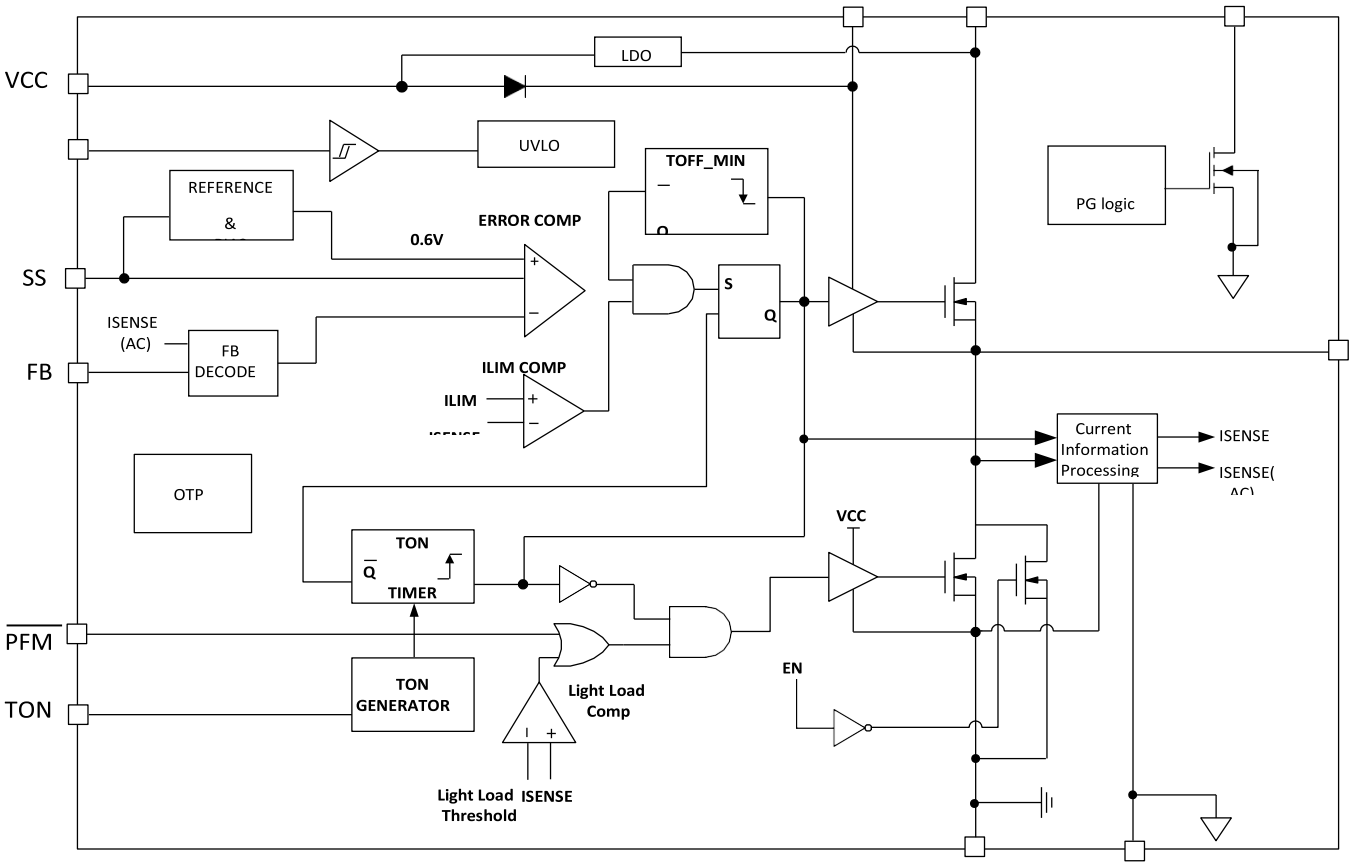
1. LX to PGND Transient (t<20ns): -7V to V_{IN} + 7V
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

3.3 Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, EN = 5V, unless otherwise specified. Specifications in BOLD indicate a temperature range of -40°C to +85°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Supply						
V_{IN}	IN Supply Voltage		**6.5**		**28**	V
V_{UVLO}	Under-Voltage Lockout Threshold	V_{CC} rising V_{CC} falling		**4.2** **3.9**		V
I_q	Quiescent Supply Current of V_{CC}	I_{OUT} = 0A, V_{EN} > 2V, PFM mode		**150**		µA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**1**	**20**	µA
V_{REF}	Feedback Voltage	T_A = 25°C T_A = 0°C to 85°C	0.594 0.591	0.6 0.6	0.606 0.609	V
I_{FB}	FB Input Bias Current				200	nA
Enable						
V_{EN}	EN Input Threshold	Off threshold On threshold	1.4		0.5	V
V_{EN_HYS}	EN Input Hysteresis			200		mV
PFM Control						
$V_{\overline{PFM}}$	$\overline{PFM}$ Input Threshold	PFM Mode threshold Force PWM threshold	2.5		0.6	V
Modulator						
T_{ON}	On Time	R_{TON} = 100kΩ, V_{IN} = 12V		200		ns
T_{ON_MIN}	Minimum On Time			100		ns
T_{ON_MAX}	Maximum On Time			3.5		µs
T_{OFF_MIN}	Minimum Off Time			300		ns
Soft-Start						
I_{SS_OUT}	SS Source Current	V_{SS} = 0V C_{SS} = 0.001µF to 0.1µF	7	11	15	µA
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			**0.5**	V
	PGOOD Leakage Current				**±1**	µA
V_{PGH}	PGOOD Threshold (Low Level to High Level)	FB rising		90		%
V_{PGL}	PGOOD Threshold (High Level to Low Level)	FB rising FB falling		120 85		
	PGOOD Threshold Hysteresis			5		
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	FB falling		50		%
V_{PH}	Over Voltage Threshold	FB rising		120		%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	V_{IN} = 12V, V_{CC} = 5V		11		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 12V, V_{CC} = 5V		4.5		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Over-current and Thermal Protection						
I_{LIM}	Current Limit	V_{CC} = 5V	45			A
	Thermal Shutdown Threshold	T_J rising T_J falling		150 125		°C

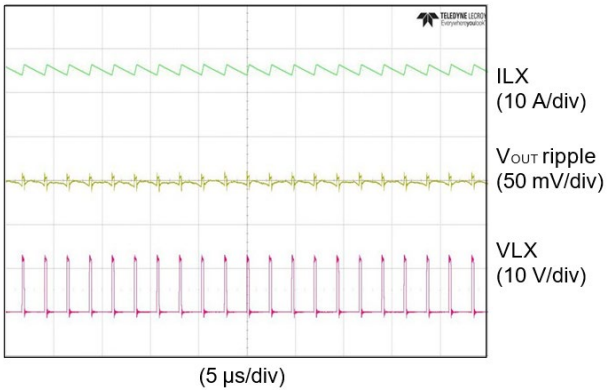
4 Functional Block Diagram



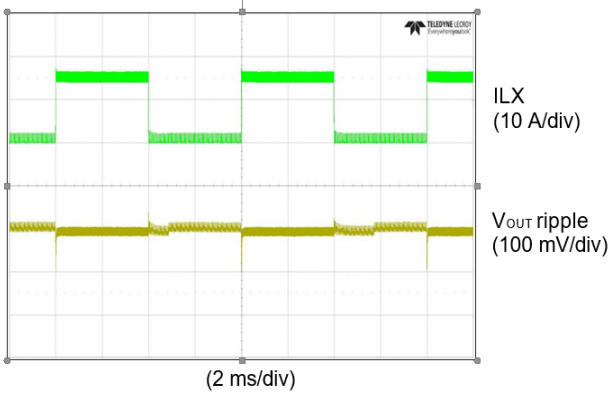
5 Typical Characteristics

T_A=25°C, V_{IN}=19V, V_{OUT}=1V, f_{sw} = 450kHz unless otherwise specified.

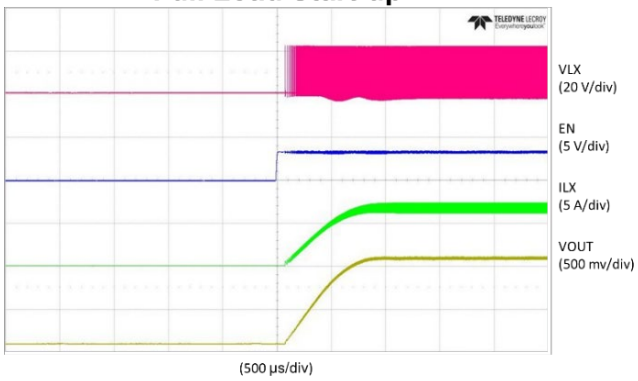
Normal Operation



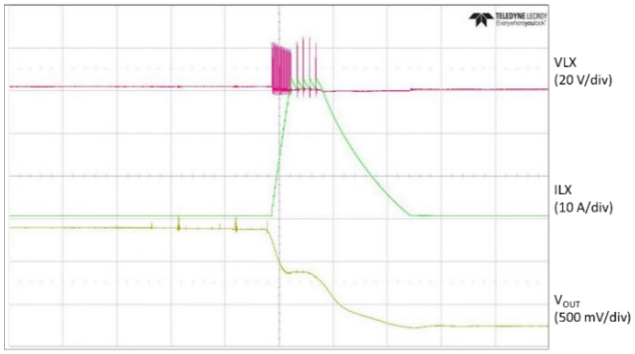
Load Transient 0A to 15A



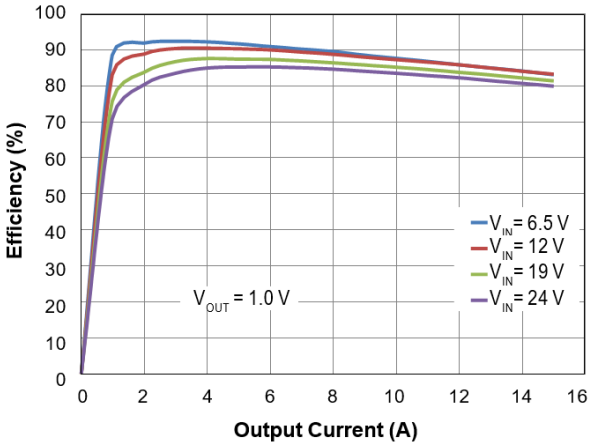
Full Load Start-up



Short Circuit Protection



Efficiency vs. Output Current



6 Functional Description & Operation

The EP6070 is a high-efficiency, easy-to-use, synchronous buck regulator optimized for notebook computers. The regulator is capable of supplying 10A of continuous output current with an output voltage adjustable down to 0.6V. The programmable on-time from 100ns to 3.5µS enables optimizing the configuration for PCB area and efficiency.

The input voltage of EP6070 can be as low as 6.5V. The highest input voltage of EP6070 can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with ceramic output capacitors. The switching frequency can be externally programmed. Protection features include V_{CC} under-voltage protection, short-circuit protection, and thermal shutdown.

The EP6070 is available in 23-pin 4 mm × 4 mm QFN package.

6.1 Input Power Architecture

The EP6070 integrates an internal linear regulator to generate 5.3V (±5%) V_{CC} from input. If input voltage is lower than 5.3V, the linear regulator operates at low drop-output mode; the V_{CC} voltage is equal to input voltage minus the drop-output voltage of internal linear regulator.

The EP6070 has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when V_{CC} rises to 4.5V and voltage on EN pin is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of soft-start pin (V_{SS}) when it is lower than 0.6V. When VSS is higher than 0.6V, the FB voltage is regulated by internal precise band-gap voltage (0.6V). When V_{SS} is higher than 3.3V, the PGOOD signal is high. The soft-start time for PGOOD can be calculated by the following formula:

$$T_{SS}(us) = 330 * C_{SS}(nF)$$

If C_{SS} is 1nF, the soft start time will be 330µs; if C_{SS} is 10nF, the soft start time will be 3.3ms.

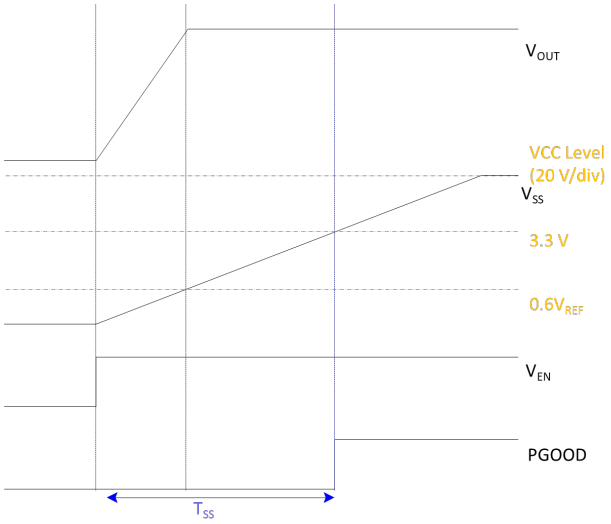


Figure 1. Soft-Start Sequence of EP6070

6.2 Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of EP6070 is constant-on-time PWM Control with input feed-forward.

The simplified control schematic is shown in Figure 2. The high-side switch on-time is determined solely by a one-shot whose pulse width can be programmed by one external resistor and is inversely proportional to input voltage (IN). The one-shot is triggered when the internal 0.6V is higher than the combined information of FB voltage and the AC current information of inductor, which is processed andobtained through the sensed lower-side MOSFET current once it turns-on. The added AC current information canhelp the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentallydifferent from other V^2 constant-on time control schemes.

The constant-on-time PWM control architecture is apseudo-fixed frequency with input voltage feed-forward. Theinternal circuit of EP6070 sets the on-time of high-sideswitch inversely proportional to the IN.

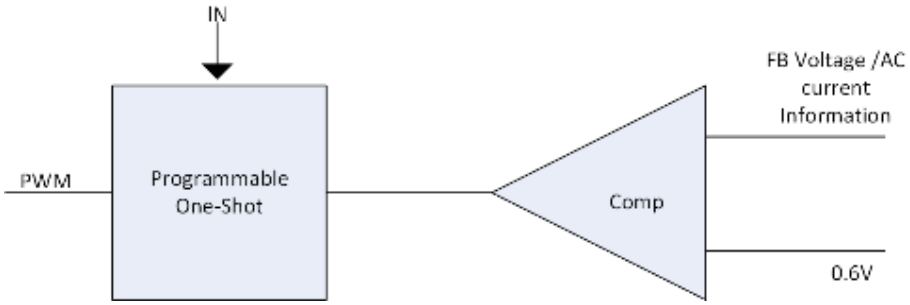


Figure 2. Simplified Control Schematic of EP6070

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of EP6070 sets the on-time of high-side switch inversely proportional to the IN.

$$T_{ON} \propto \frac{R_{TON}\ (\Omega)}{V_{IN}(V)}$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}}$$

Once the product of V_{IN} x T_{ON} is constant, the switching frequency keeps constant and is independent with input voltage.

An external resistor between the IN and TON pin sets the switching on-time according to the following curves:

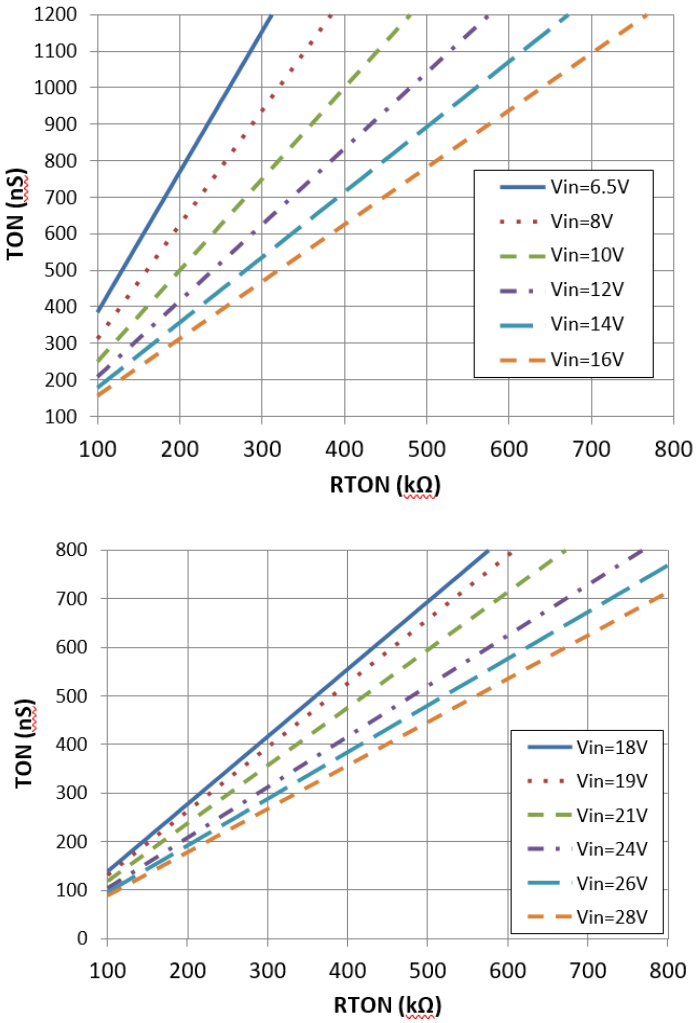


Figure 3. T_{ON} vs. R_{TON} Curves for EP6070

A further simplified equation will be:

$$F_{SW}(kHz) = \frac{V_{OUT}\ (V)}{V_{IN}\ (V) \times T_{ON}\ (ns)} \times 10^6$$

If V_{OUT} is 1.05V, V_{IN} is 19V, and set F_{SW}=500kHz. According to eq. (3), T_{ON}=110nS is needed. Finally, use the T_{ON} to R_{TON} curve, we can find out R_{TON} is 82kΩ.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

6.3 Output Voltage Control (DAC)

if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The EP6070 senses the low-side MOSFET current and processes it into DC current and AC current information using proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's

ESR. Thus, the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

6.4 Current-Limit Protection

The EP6070 has the current-limit protection by using RDSON of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off (300ns typical) is implemented after a constant-on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 64 switching cycles, the EP6070 considers this is a true failed condition and thus turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the EP6070 again.

6.5 Output Voltage Under-Voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, EP6070 will turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the EP6070 again.

6.6 Output Voltage Over-Voltage Protection

The threshold of OVP is set 20% higher than 0.6V. When the VFB voltage exceeds the OVP threshold, high-side MOSFET is turn-off and low-side MOSFETs is turn-on 1 µS, then latch-off.

6.7 Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 15% below than the nominal regulation voltage for, the PGOOD is pulled low. When the output voltage is 20% higher than the nominal regulation voltage, the PGOOD is also pull low.

When combined with the under-voltage-protection circuit, this current-limit method is effective in almost every circumstance.

7 Application Information

The basic EP6070 application circuit is shown in the first page. Component selection is explained below.

7.1 Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the EP6070 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7µF, should be connected to the V_{CC} pin and AGND pin for stable operation of the EP6070. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$V_{IN} = \frac{I_{OUT}\,(V)}{f \times C_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times \frac{V_{OUT}}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}(1 - \frac{V_{OUT}}{V_{IN}})}$$

if let m equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 4. It can be seen that when VOUT is half of V, CIN is under the worst current stress. The worst current stress on CIN is 0.5 x IOUT.

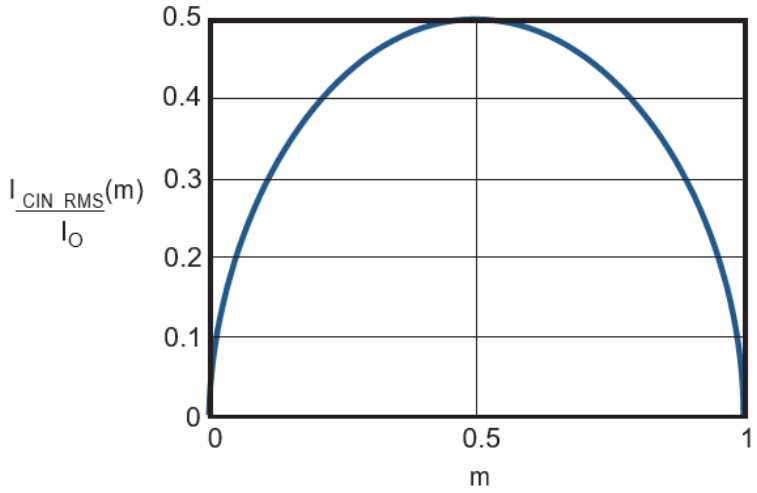


Figure 4. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than ICIN_RMS at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also

be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of lifetime. Further de-rating may be necessary for practical design requirement.

7.2 Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.
When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

7.3 Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.
The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.
Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times (ESR_{CO} + \frac{1}{8 \times f \times C_{OUT}})$$

where, C_O is output capacitor value, and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$V_{OUT} = \Delta I_L \times \frac{1}{8 \times f \times C_{OUT}}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$V_{OUT} = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak-to-peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

8 Thermal Management and Layout Consideration

In the EP6070 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In the PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the EP6070.

In the EP6070 buck regulator circuit, the major power dissipating components are the EP6070 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power. The power dissipation of inductor can be approximately calculated by output current and DCR of inductor and output current.

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{total\_loss} = V_{IN} \cdot I_{IN} - I_{OUT} \cdot V_{OUT}$$

The actual junction temperature can be calculated with power dissipation in the EP6070 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor_{loss}}) \cdot \Theta_{JA} + T_A$$

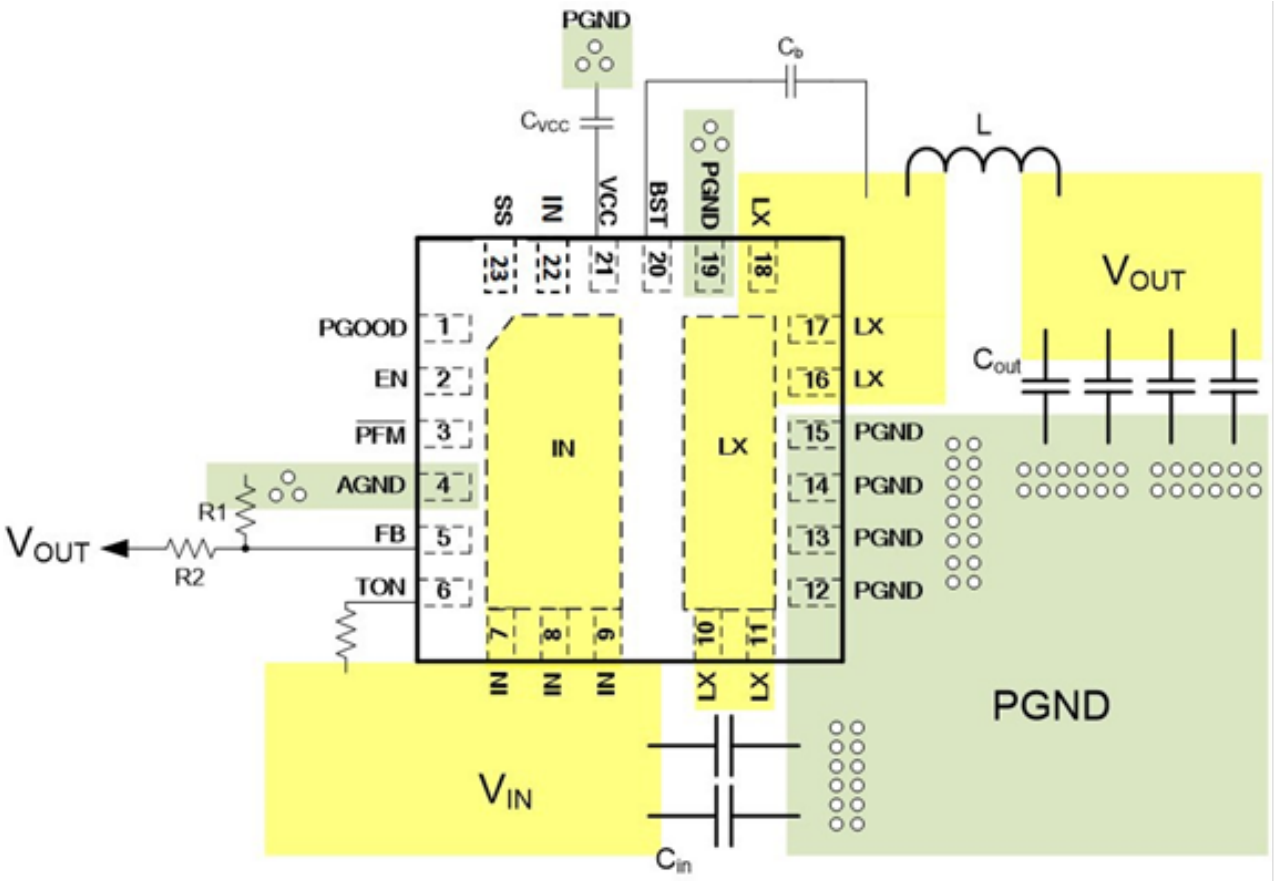
The maximum junction temperature of EP6070 is 150ºC, which limits the maximum load current capability.

The thermal performance of the EP6070 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

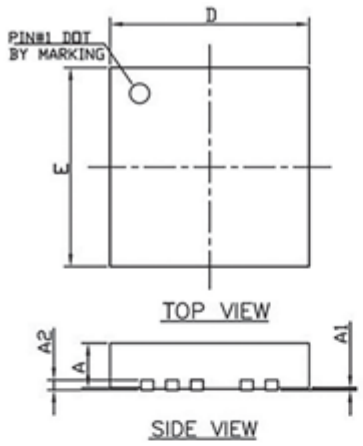
8.1 Layout Considerations

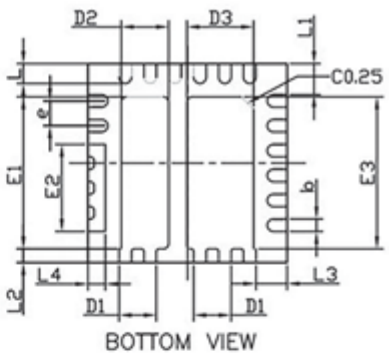
Several layout tips are listed below for the best electric and thermal performance.

1. The LX pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connect a large copper plane to LX pin to help thermal dissipation.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor CV_{CC} should be connected to V_{CC} and AGND as close as possible.
5. Voltage divider R1 and R2 should be placed as close as possible to FB and AGND.
6. RTON should be connected as close as possible to Pin 6 (TON pin).
7. A ground plane is preferred; Pin 19 (PGND) must be connected to the ground plane through via.
8. Keep sensitive signal traces such as feedback trace far away from the LX pins.
9. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
10. Place via to connect AGND pin and ground layer, the via must be placed as close as possible to AGND pin. Place via as close as possible to PGND pins and the ground side of output capacitor, too.



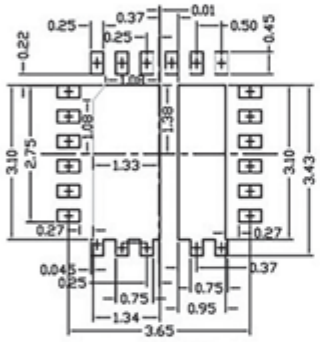
9 Package Dimensions, QFN 4x4-23L



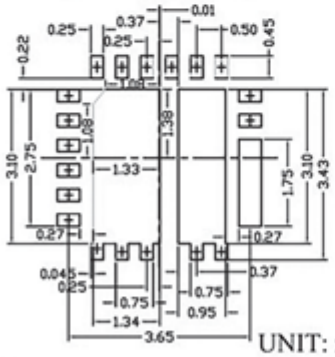


RECOMMENDED LAND PATTERN

Option 1



Option 2



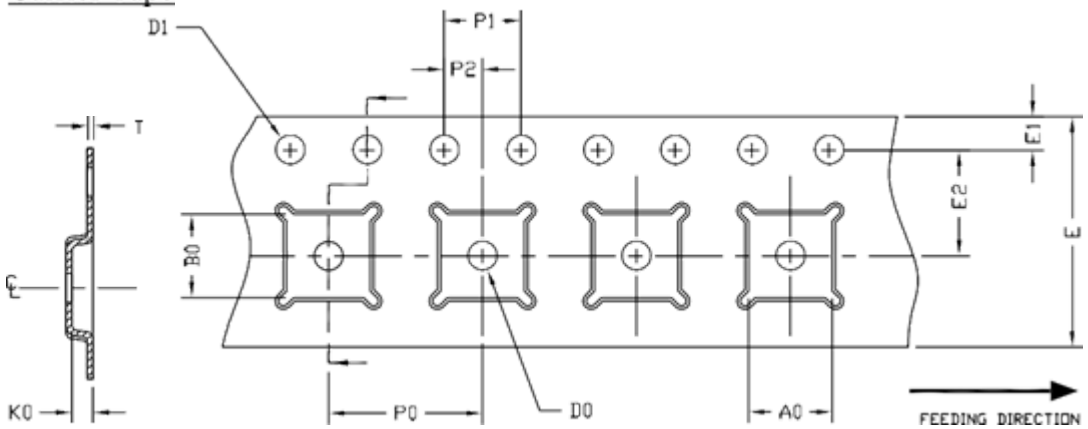
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	——	0.05	0.000	——	0.002
A2		0.2 REF			0.008 REF	
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.65	1.75	1.85	0.065	0.069	0.073
E3	2.95	3.05	3.15	0.116	0.120	0.124
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.034
D2	0.85	0.95	1.05	0.033	0.037	0.041
D3	1.24	1.34	1.44	0.049	0.053	0.057
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
L3	0.57	0.62	0.67	0.022	0.024	0.026
L4	0.30	0.35	0.40	0.012	0.014	0.016
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020 BSC	

UNIT: mm

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: ±0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

10 Tape and Reel Dimensions, QFN 4x4-23L

Carrier Tape

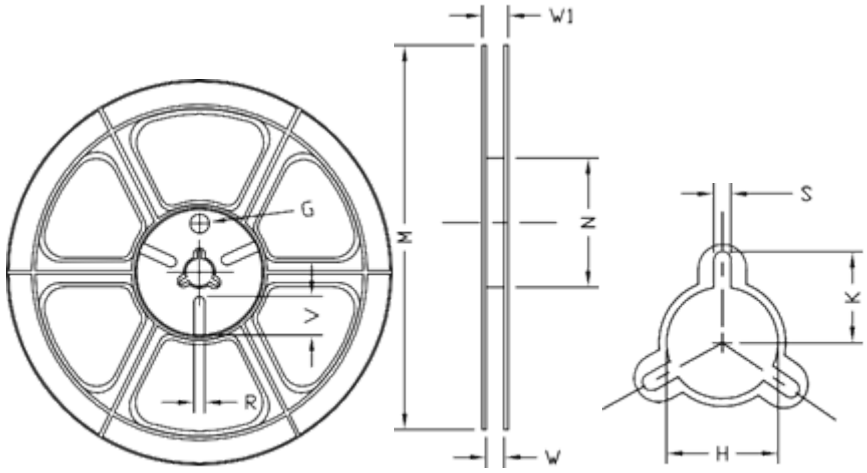


Reel

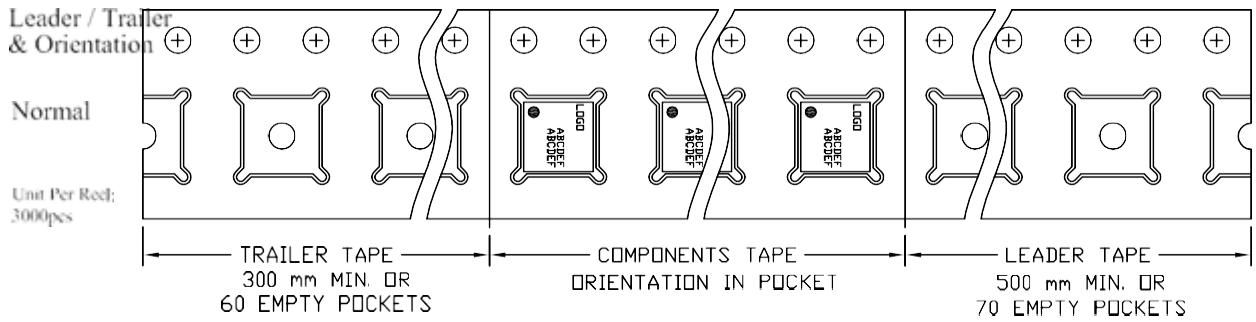
UNIT MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel



Tape


Leader / Trailer
& Orientation
Normal
Unit Per Reel:
3000pcs
TRAILER TAPE
300 mm MIN. OR
60 EMPTY POCKETS
COMPONENTS TAPE
ORIENTATION IN POCKET
LEADER TAPE
500 mm MIN. OR
70 EMPTY POCKETS

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