MULTI-FUNCTIONALITY OF GPIOS IN EP71XX

AN-EP71xx-2

EMPOWER SEMICONDUCTOR, INC.

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1. Table of Contents

Multi-functionality of GPIOs

2. Overview

Empower Semiconductor's EP71xx series is a family of Step-Down Integrated voltage regulators (IVRs) available in single to quad-output configurations. The EP71xx features two user-programmable general-purpose inputs/outputs (GPIO0, GPIO1) which can be configured to perform various functions. This application note provides details on configuring and utilizing the GPIOs through examples.

Refer to EP71xx Product Description document and Device datasheet for details on the features, electrical characteristics, and functional description of the product family.

3. Programming the multi-functions of GPIOs

GPIO0 and GPIO1 in the EP71xx pins are programmable IOs that can be configured to perform various functions such as dynamic voltage scaling control input (DVS), alternate power good output (ALT PG), alert output (GPIO ALERT) or enable input (Hardware EN).

3.1 User Programmable Registers for GPIO Programming

Table 1 shows the list of user-programmable registers for programming the GPIOs. Each of these registers is further explained in detail in this section through examples.

Register Name (User-programmable registers)	Bits	Reg Address
GPIO_ALERTS - Table 7	[6:0]	0x22
GPIO0_FUNCTION - Table 8	[6:4]	0x23
GPIO0_VRS - Table 8	[3:0]	
GPIO1_FUNCTION - Table 9	[6:4]	0x24
GPIO1_VRS - Table 9	[3:0]	

Table 1: User-Programmable Registers table for GPIO programming

GPIOx_FUNCTION registers (Table 8, Table 9) set the GPIO function for the selected VR rails defined through the **GPIOx_VRS** registers (Table 7). The GPIOs can perform the below functions:

- **Dynamic Voltage Scaling (DVS) Function**
- **Alternate Power Good**
- **Hardware Enable**
- **GPIO Alert**

3.2 GPIOs as 'DVS' Input

GPIO0/GPIO1 can be set as an input to trigger DVS on the VR included in **GPIO_VRS**. The **VRn_SLEW_RATE_UP, VRn_SLEW_RATE_DOWN** registers, shown in Table 10, set the DVS (dynamic output voltage) slew rate up and down respectively for the relevant VR*n* (where *n* is a number from 1 to 4 which represents the VR number VR1, ….VR4 for EP71xx). Set **VRn_SLEW_RATE_UP** or **VRn_SLEW_RATE_DOWN** to 0x0 for the slowest possible slew rate. Set these register bits to 0x0F for the fastest possible slew rate. Refer to Table 12 for details.

If a **GPIO_VRS** bit is configured for GPIO0 and GPIO1, GPIO0 takes precedence. **VRn_DAC_TARGET** and **VRn_DAC_TARGET2** registers are used to set the two voltage levels for DVS (Table 13).

In **Figure 1** and **Figure 2**, GPIO0 is the DVS input to VR1 and VR3. When GPIO0 is set HI, DVS between **VRn_DAC_TARGET** to **VRn_DAC_TARGET2** takes place and vice-versa when GPIO0 is pulled LOW.

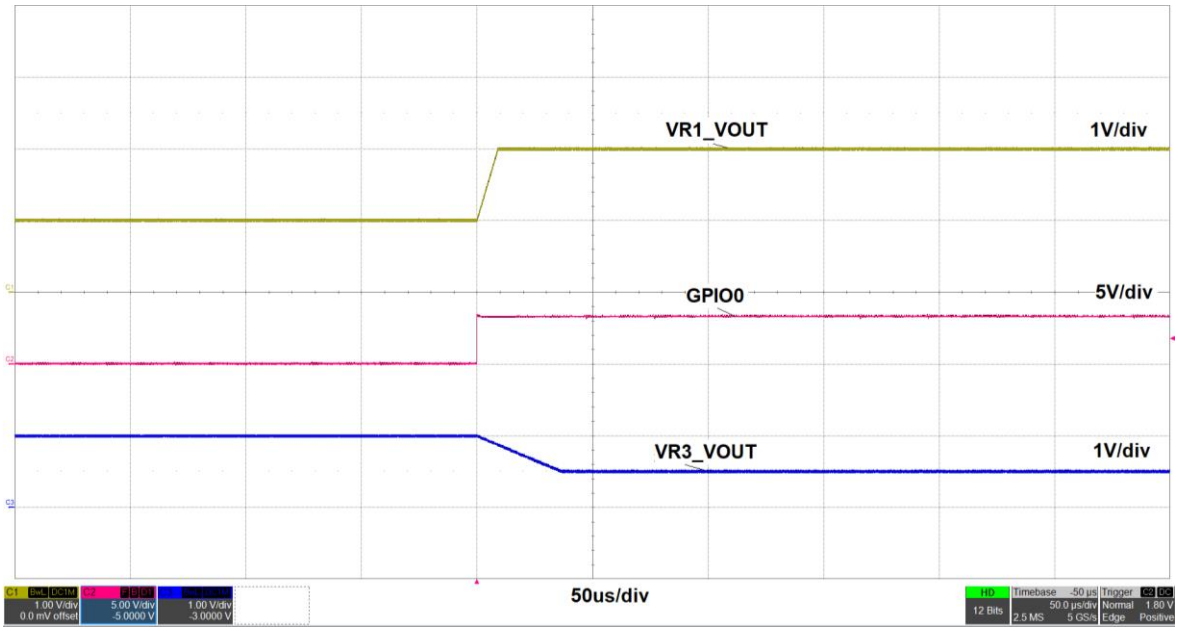

Figure 1. GPIO0 configured as DVS in EP7144, DVS-Up

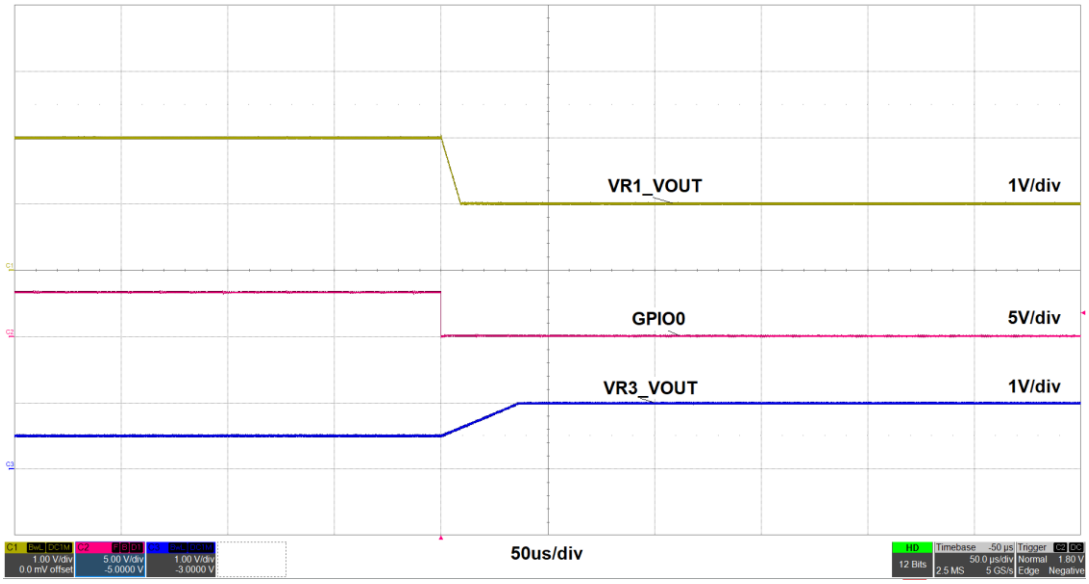

Figure 2. GPIO0 configured as DVS in EP7144, DVS-Down

Bit field Name	Register Address	Bits	Setting	Description of changes
VR1_DAC_TARGET	0x41	[1:0]	0x19A	Sets VR1 Output Voltage to 1V
	0x42	[7:0]		
VR1_DAC_TARGET2	0x43	[1:0]	0x334	Sets VR1 Output Voltage to 2V
	0x44	[7:0]		
VR3_DAC_TARGET	0x61	[1:0]	0x19A	Sets VR3 Output Voltage to 1V
	0x62	[7:0]		
VR3_DAC_TARGET2	0x63	[1:0]	0xCD	Sets VR3 Output Voltage to 0.5V
	0x64	[7:0]		
VR1_SLEW_RATE_UP	0x46	[7:4]	0x0B	VR1 Slew rate up/down setting
VR1_SLEW_RATE_DOWN		[3:0]	0x0B	
VR3_SLEW_RATE_UP	0x66	[7:4]	0x0B	VR3 Slew rate up/down setting
VR3_SLEW_RATE_DOWN		[3:0]	0x0B	
GPIO0_FUNCTION	0x23	[6:4]	0x00	GPIO0 set as DVS Input
GPIO0_VRS		[3:0]	0x05	GPIO0 set as DVS IN for VR1, VR3
VR1_ENABLE	0x20	[0]	1	Enable VR1
VR3_ENABLE		[2]	1	Enable VR3
EXECUTE	0x0F	[7:0]		Write any value to the register to apply register settings
Toggle GPIO0 - Toggle GPIO0 HI or LO to observe DVS transitions				

*Table 2: GPIO0 as DVS-Input - **Figure 1, Figure 2***

3.3 GPIOs as 'Alternate Power Good'

The GPIO can function as Power Good output, an alternate to the PG pin on the device, such that it asserts HI for the VRs included in **GPIO_VRS**.

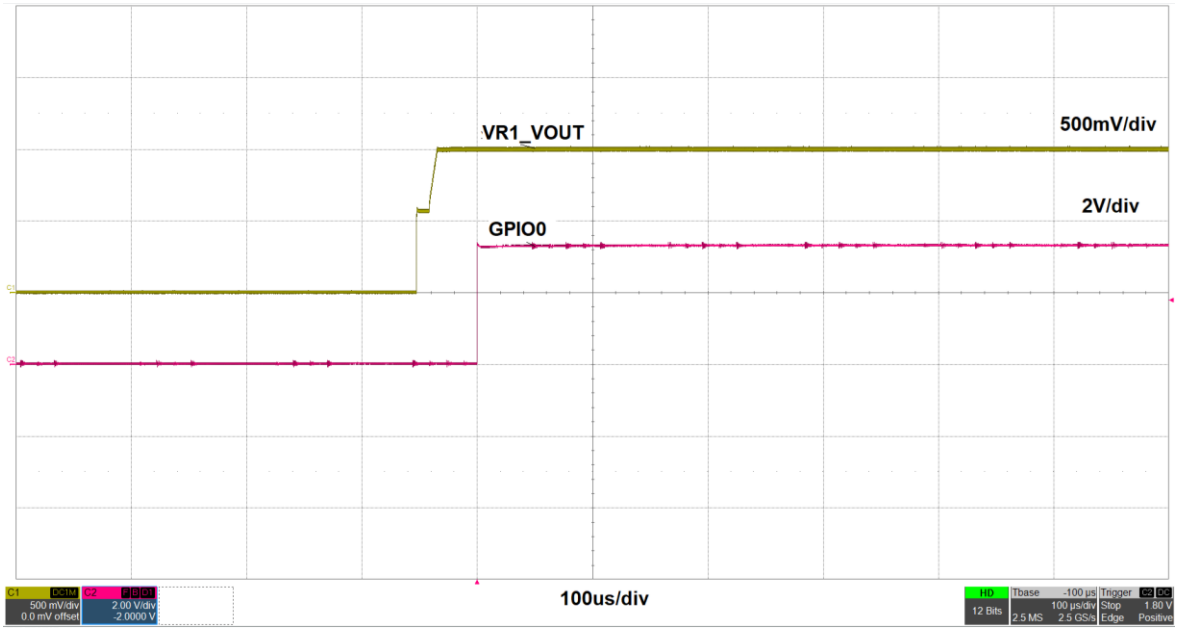

Figure 3. GPIO0 configured as 'Alt PG' in EP7144

In **Figure 3**, GPIO0 functions as PG output for VR1. When VR1 reaches regulation at the desired output voltage, GPIO0 asserts HI.

Bit field Name	Register Address	Bits	Setting	Description of changes
VR1_DAC_TARGET	0x41	[1:0]	0x19A	Sets VR1 Output Voltage to 1V
	0x42	[7:0]		
GPIO0_FUNCTION	0x23	[6:4]	0x01	GPIO0 set as 'Power Good' Output
GPIO0_VRS		[3:0]	0x01	GPIO0 set as PG OUT for VR1
VR1_ENABLE	0x20	[0]	1	Enable VR1
EXECUTE	0x0F	[7:0]		Write any value to the register to apply register settings

*Table 3: GPIO0 as PG Output - **Figure 3***

3.4 GPIOs as 'GPIO Alert'

GPIOs of EP71xx can be configured as alerts to indicate the occurrence of the events such as over-temperature, input undervoltage, input overvoltage, VR output undervoltage, VR output overvoltage and VR output short circuit by enabling the GPIO Alert functions (listed in Table 7). Alerts enabled will cause the GPIO to assert HI when the fault occurs.

For the Alert functions that are applicable to the VRs, **GPIOn_VRS** register in Table 7 indicates the specific VR being monitored for faults. The two GPIOs can be pointed at different VRs for the VR-focused alerts. Refer to the product datasheet for further details.

In the example below, GPIO0 monitors VR1 for the occurrence of a short circuit condition. In a short circuit event on VR1, GPIO0 is pulled HI indicating a short circuit event. VR1 attempts to recover but fails due to the continuing short condition. GPIO0 follows the VR1 output voltage.

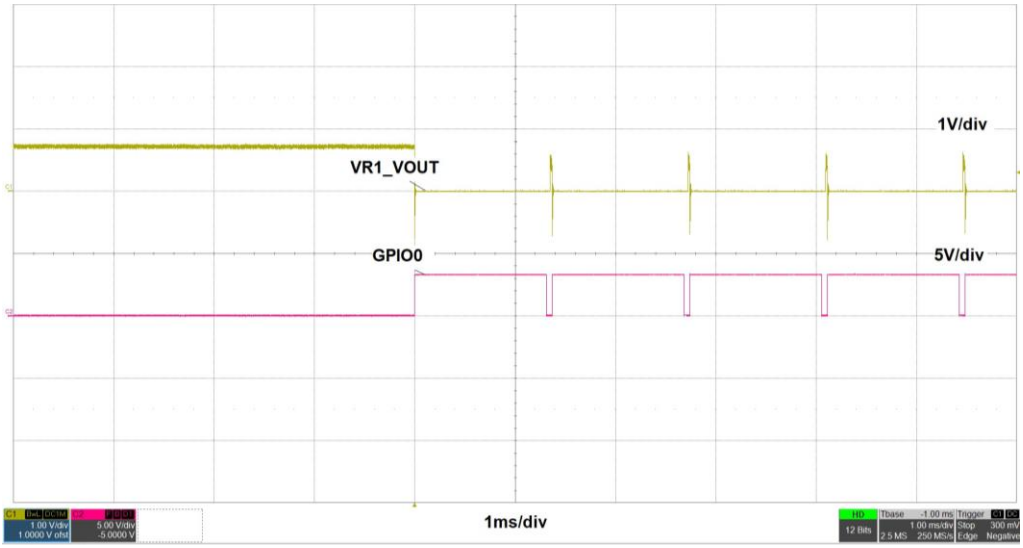

Figure 4. GPIO0 configured as 'GPIO Alert' in EP7144. GPIO0 is set to monitor VR1 Output short-circuit fault.

Bit field Name	Register Address	Bits	Setting	Description of changes
VR1_DAC_TARGET	0x41	[1:0]	0x19A	Sets VR1 Output Voltage to 1V
	0x42	[7:0]		
GPIO0_FUNCTION	0x23	[6:4]	0x02	GPIO0 set as 'GPIO Alert'
GPIO0_VRS		[3:0]	0x01	GPIO0 set as Alert for fault in VR1
GPIO_ALERT	0x22	[7:0]	0x01	GPIO configured to detect output short circuit condition on selected VR.
VR1_ENABLE	0x20	[0]	1	Enable VR1
EXECUTE	0x0F	[7:0]		Write any value to the register to apply register settings

*Table 4: GPIO0 as PG Output - **Figure 3***

3.5 GPIOs as 'Hardware Enable'

GPIO can be configured as a HW Enable for the VRs indicated in **GPIO_VRS**.

Note:

- It is possible to configure GPIO0 and GPIO1 as HW enables for one rail. In this case, either of the GPIOs can start the rail.
- The VR that has been enabled will power up with a default chip enable delay. Additional delay can be included in the startup of the VR through the delay register bits (refer to EP71xx datasheet).
- When a GPIO is configured to act as HW Enable for a VRn, the corresponding **VRn_ENABLE** register bit (Table 6) is not set to 1. The **VRn_ENABLE** register bits and the HW Enable functions are logically OR'ed. The VRn can be disabled only by pulling the GPIO voltage low, or by disabling the device (Chip Enable is disabled).

In the example below (**Figure 5** and **Figure 6**), GPIO0 is programmed as HW Enable for VR1. When GPIO0 is pulled HI, this enables VR1 which in turn triggers the power-up sequence (VR3 and VR4 are enabled through start conditions). When GPIO0 is pulled low, the power-down sequence is initiated.

3.5.1 Power-up sequence Initiated by GPIO Enable

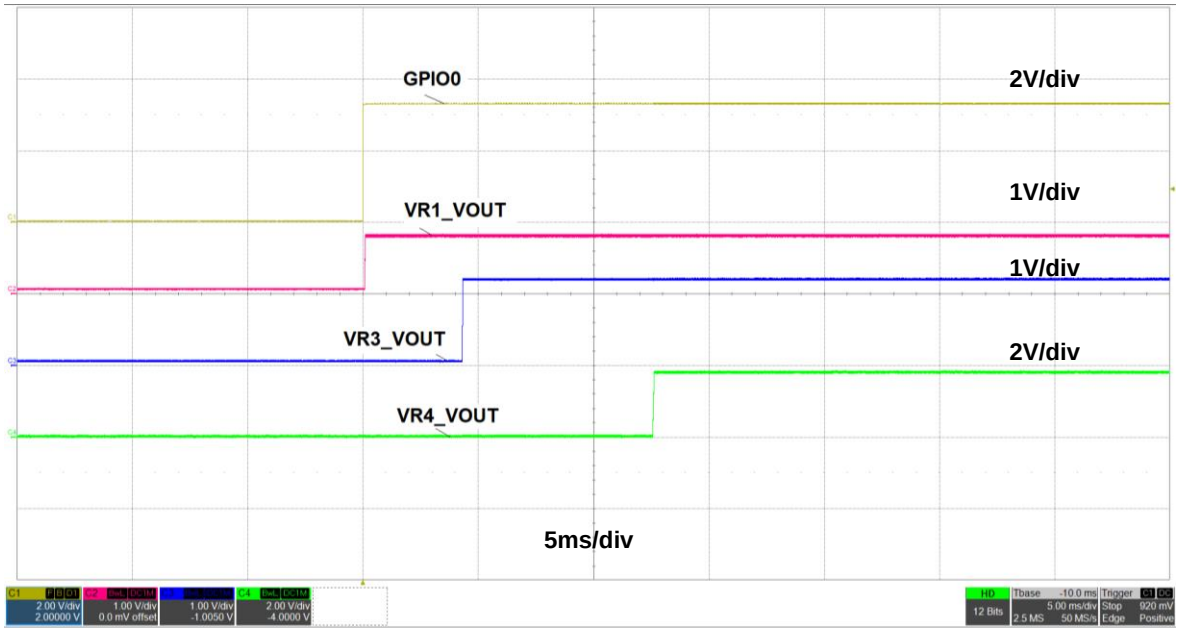

Figure 5. GPIO0 configured as Hardware Enable in EP7143. Waveforms showing power-up sequence triggered on GPIO0 = HIGH

3.5.2 Power-down sequence when GPIO disabled

Figure 6. Example: Waveforms showing power-down sequence triggered on GPIO0 = LOW

Bit field Name	Register Address	Bits	Reg Setting (hex)	Description of changes
VR1_DAC_TARGET	0x41	[1:0]	0x148	Sets VR1 Output Voltage to 0.8V
	0x42	[7:0]		
VR3_DAC_TARGET	0x61	[1:0]	0x1EC	Sets VR3 Output Voltage to 1.2V
	0x62	[7:0]		
VR4_DAC_TARGET	0x71	[1:0]	0x2E2	Sets VR4 Output Voltage to 1.8V
	0x72	[7:0]		
VR1_ENABLE	0x20	[0]	0	Default settings
VR3_ENABLE		[2]	0	Default settings
VR4_ENABLE		[3]	0	Default settings
GPIO0_FUNCTION	0x23	[6:4]	0x04	GPIO0 set as HW Enable
GPIO0_VRS		[3:0]	0x01	GPIO0 set HW EN for VR1
VR1_DELAY_UP	0x25	[7]	0	- No delay during power-up
VR1_DELAY_DOWN		[6]	1	- Delay applied during power-down
VR1_START_CONDITION		[5:3]	0x00	- No start condition
VR1_HOLD_CONDITION		[2:0]	0x02	- Shut down of Rail VR1 dependent on shutdown of Rail VR3
VR1_DELAY	0x26	[7:0]	0x2C	Sets delay time ~4ms
VR3_DELAY_UP	0x29	[7]	1	- Delay applied during power-up and power-down
VR3_DELAY_DOWN		[6]	1	- Startup of Rail VR3 dependent on startup of Rail VR1
VR3_START_CONDITION		[5:3]	0x01	
VR3_HOLD_CONDITION		[2:0]	0x04	- Shut down of Rail VR3 dependent on shutdown of Rail VR4
VR3_DELAY	0x2A	[7:0]	0x2C	Sets delay time ~4ms
VR4_DELAY_UP	0x2B	[7]	1	Delay applied during power-up and power-down
VR4_DELAY_DOWN		[6]	1	- Startup of Rail VR4 dependent on startup of Rail VR3
VR4_START_CONDITION		[5:3]	0x04	
VR4_HOLD_CONDITION		[2:0]	0x00	- No hold condition. Shut down of Rail VR4 dependent on GPIO0 disable. (GPIO0 set low).
VR4_DELAY	0x2C	[7:0]	0x58	Sets delay time ~8ms
EXECUTE	0x0F	[7:0]		Write any value to apply register settings
Toggle GPIO0 - Toggle GPIO0 HI or LO to observe DVS transitions				

*Table 5: Register settings for **Figure 5** and **Figure 6***

4. Appendix

4.1 VR Enable Registers

Reg Address	Bits	Bit Field Name	Read/ Write	Reset Value	Description
0x20	7	NA	R/W	0x00	Not used
	6	NA			Not used
	5	NA			Not used
	4	NA			Not used
	3	VR4_ENABLE			Write to this register during normal operation to control the state of a VR output. Write 1 to enable VRn. Write 0 to disable VRn.
	2	VR3_ENABLE			
	1	VR2_ENABLE			
	0	VR1_ENABLE			

Table 6: VR Enable Register

4.2 GPIO Alert Registers

Reg Address	Bits	Bit Field Name	Read/ Write	Reset Value (hex)	Description
0x22	7	NA	R/W	0x00	Not used
	6	GPIO_ALERT_OT			Over Temperature alert: When the die temperature is above the over-temperature warning threshold, the configured GPIO asserts high. PG is de-asserted.

	5	GPIO_ALERT_UV			Input Undervoltage alert: When the Input voltage is below the input under-voltage warning threshold ($V_{PVIN\_REG\_UV\_WARN\_THR}$), the configured GPIO asserts high. PG is de-asserted.
	4	GPIO_ALERT_OV			Input Overvoltage alert: When the Input voltage is above the input over-voltage warning threshold ($V_{PVIN\_REG\_OV\_WARN\_THR}$), the configured GPIO asserts high. PG is de-asserted.
	2	GPIO_ALERT_VLOW			VR Output Undervoltage alert: The configured GPIO asserts high if the output voltage of the VR specified in GPIO_VRS falls below the output undervoltage warning threshold (15% below the target voltage). PG is de-asserted.
	1	GPIO_ALERT_VHIGH			VR Output Overvoltage alert: The configured GPIO asserts high if the output voltage of the VR specified in GPIO_VRS exceeds the output overvoltage warning threshold (15% above the target voltage). PG is de-asserted.
	0	GPIO_ALERT_SHORT			VR short-circuit alert: The configured GPIO asserts high if the VR specified in GPIO_VRS detects an output short circuit condition. PG is de-asserted.

Table 7: GPIO Alerts Register

4.3 GPIO Functions Registers

Reg Address	Bits	Bit Field Name	Read/ Write	Reset Value (hex)	Function/Description			
					GPIO Setting	Function	Input/ Output	Description
0x23	[7]	NA	R/W	0x00	NA	NA	NA	Not used

	[6:4]	GPIO0_FUNCTION			000	DVS Function	Input	This allows to set GPIO0 as an input for DVS Function. The logic state of the GPIO is fed to the DVSIN signals to each VR included in GPIOx_VRS (If a GPIO_VRS bit is configured for both GPIO0 and GPIO1, GPIO0 takes precedence). The LOW state selects the voltage programmed in VRn_DAC_TARGET register and the HIGH state selects the voltage programmed in VRn_DAC_TARGET2 register.
					001	Alt PG	Output	GPIO programmed to function as Power Good. GPIO asserts high when all VRs included in GPIO_VRS are in regulation and output voltage has stabilized.
					010	GPIO Alert	Output	Allows GPIOx to be used as an output for alert functions for the VRs included in GPIOx_VRS will cause the GPIO to assert high.
					1xx	HW Enable	Input	Bit 6 sets GPIO0 as input to serve as a HW enable for the VRs indicated by GPIOx_VRS. It can be configured as a HW Enable for one or all VRs.
	[3:0]	GPIO0_VRS			GPIO0 Functions apply to VR4 (Bit 3 is set for VR4)			
					GPIO0 Functions apply to VR3 (Bit 2 is set for VR3)			
					GPIO0 Functions apply to VR2 (Bit 1 is set for VR2)			
					GPIO0 Functions apply to VR1 (LSB is set for VR1)			

Table 8: GPIO0 Functions Register

Reg Address	Bits	Bit Field Name	Read/ Write	Reset Value (hex)	Function/Description			
					GPIO Setting	Function	Input/ Output	Description
0x24	[7]	NA	R/W	0x00	NA	NA	NA	Not used

	[6:4]	GPIO1_FUNCTION			000	DVS Function	Input	This allows to set GPIO1 as an input for DVS Function. The logic state of the GPIO is fed to the DVSIN signals to each VR included in GPIOx_VRS (If a GPIO_VRS bit is configured for both GPIO0 and GPIO1, GPIO0 takes precedence). The LOW state selects the voltage programmed in VRn_DAC_TARGET register and the HIGH state selects the voltage programmed in VRn_DAC_TARGET2 register.
					001	Alt PG	Output	GPIO programmed to function as Power Good. GPIO asserts high when all VRs included in GPIO_VRS are in regulation and output voltage has stabilized.
					010	GPIO Alert	Output	Allows GPIO1 to be used as an output for alert functions for the VRs included in GPIOx_VRS will cause the GPIO to assert high.
					1xx	HW Enable	Input	Bit 6 sets GPIO as input to serve as a HW enable for the VRs indicated by GPIOx_VRS. It can be configured as a HW Enable for one or all VRs.
	[3:0]	GPIO1_VRS			GPIO1 Functions apply to VR4 (Bit 3 is set for VR4)			
					GPIO1 Functions apply to VR3 (Bit 2 is set for VR3)			
					GPIO1 Functions apply to VR2 (Bit 1 is set for VR2)			
					GPIO1 Functions apply to VR1 (LSB is set for VR1)			

Table 9: GPIO1 Functions Register

4.4 DVS Ramp Rate Registers

Reg Address	Bits	Bit Field Name	Read/ Write	Reset Value (hex)	Description

0x46	[7:4]	VR1_ SLEW_RATE_UP	R/W	0x0A	DVS ramp up slew rate control register: The value in this register sets the DVS Ramp Up slew Rate for VR1.
	[3:0]	VR1_ SLEW_RATE_DOWN		0x0A	DVS ramp down slew rate control register: The value in this register sets the DVS Ramp Down slew Rate for VR1.
0x56	[7:4]	VR2_ SLEW_RATE_UP	R/W	0x0A	DVS ramp up slew rate control register: The value in this register sets the DVS Ramp Up slew Rate for VR2.
	[3:0]	VR2_ SLEW_RATE_DOWN		0x0A	DVS ramp down slew rate control register: The value in this register sets the DVS Ramp Down slew Rate for VR2.
0x66	[7:4]	VR3_ SLEW_RATE_UP	R/W	0x0A	DVS ramp up slew rate control register: The value in this register sets the DVS Ramp Up slew Rate for VR3.
	[3:0]	VR3_ SLEW_RATE_DOWN		0x0A	DVS ramp down slew rate control register: The value in this register sets the DVS Ramp Down slew Rate for VR3.
0x76	[7:4]	VR4_ SLEW_RATE_UP	R/W	0x0A	DVS ramp up slew rate control register: The value in this register sets the DVS Ramp Up slew Rate for VR4.
	[3:0]	VR4_ SLEW_RATE_DOWN		0x0A	DVS ramp down slew rate control register: The value in this register sets the DVS Ramp Down slew Rate for VR4.

Table 10: VR DVS Ramp Rate Registers

The DVS slew rate for a given part number falls into one of two categories: Rate A or Rate B. The table below shows the categories by part number:

Part Number	Slew Rate
EP7112, EP7123, EP7136, EP7143	A
EP7124, EP7131, EP7139, EP7144	B

Table 11: Part Number vs Category A/B

The register bit field **VRn_SLEW_RATE_UP/DOWN** setting vs expected DVS Slew Rate is listed in **Table 12.**

VRn_SLEW_RATE_UP/DOWN (code setting)	DVS Slew Rate A (mV/µs)	DVS Slew Rate B (mV/µs)
0	0.05	0.12

1	0.11	0.235
2	0.22	0.46
3	0.43	0.94
4	0.9	1.86
5	1.72	3.47
6	3.5	6.92
7	7	13.8
8	14	27.4
9	27	54.4
10	54	109
11	110	216
12	220	430
13	450	860
14	900	1400

Table 12: Output DVS Slew Rate Settings

4.5 VR Output Voltage Registers

The output voltage control registers set the target output voltage for the corresponding VR between 0.5V and 2.5V as shown in **Table 13**.

Reg Address	Bits	Bit Field Name	Read/Write	Reset Value (hex)	Description
0x41	[7:2]	NA	R/W	0x00	Sets the VRn target output voltage. VOUTn = ([VRn_DAC_TARGET]DECIMAL/410), where VOUTn is the VRn target output voltage.
	[1:0]	VR1_DAC_TARGET_MSB		0x199	
0x42	[7:0]	VR1_DAC_TARGET_LSB			
0x43	[7:2]	NA		0x00	

	[1:0]	VR1_DAC_TARGET2_MSB		0x00	Write to VRn_DAC_TARGET to set the VRn output voltage between 0.5V (0xCD) and 2.495V (0x3FF), where n is a number between 1 and 4 representing the VR number (VR1, VR2, VR3 and VR4). If DVS function is enabled, final DAC target value is assigned to DAC_TARGET2.
0x44	[7:0]	VR1_DAC_TARGET2_LSB			
0x51	[7:2]	NA	R/W	0x00	
	[1:0]	VR2_DAC_TARGET_MSB		0x199	
0x52	[7:0]	VR2_DAC_TARGET_LSB			
0x53	[7:2]	NA		0x00	
	[1:0]	VR2_DAC_TARGET2_MSB		0x00	
0x54	[7:0]	VR2_DAC_TARGET2_LSB			
0x61	[7:2]	NA	R/W	0x00	
	[1:0]	VR3_DAC_TARGET_MSB		0x199	
0x62	[7:0]	VR3_DAC_TARGET_LSB			
0x63	[7:2]	NA		0x00	
	[1:0]	VR3_DAC_TARGET2_MSB		0x00	
0x64	[7:0]	VR3_DAC_TARGET2_LSB			
0x71	[7:2]	NA	R/W	0x00	
	[1:0]	VR4_DAC_TARGET_MSB		0x199	
0x72	[7:0]	VR4_DAC_TARGET_LSB			
0x73	[7:2]	NA		0x00	
	[1:0]	VR4_DAC_TARGET2_MSB		0x00	
0x74	[7:0]	VR4_DAC_TARGET2_LSB			

Table 13: VR Output Voltage Registers

5. Revision History

#	Date	Description	Version
1.	Jan 8, 2024	Initial version released.	1.0
2.	Feb 7, 2024	Formatting Updated	1.1