INPUT SOURCE IMPEDANCE CONSIDERATIONS FOR EP71XX

AN-EP71xx-3

EMPOWER SEMICONDUCTOR, INC.

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Input Source Impedance Considerations

2. Overview

The EP71xx family of integrated voltage regulators (IVR) do not require any external components. However, the impedance of the source voltage – both DC and over frequency – must be properly controlled to maintain voltage stability at the IVR input. Also, dynamic behavior, such as fast dynamic voltage scaling (DVS) or transient loading may cause the EP71xx input voltage to change due to the interaction of the input current with the input source impedance. Thus, proper selection of the steady-state and dynamic input source impedance is critical for getting the highest performance from the EP71xx products.

Figure 1 shows the EP71xx IVR and its input supply modeled as an ideal voltage source, V_S, followed by series resistance, R, and series inductance, L, representing the PDN, and integrated input bypass capacitor C_{IN}.

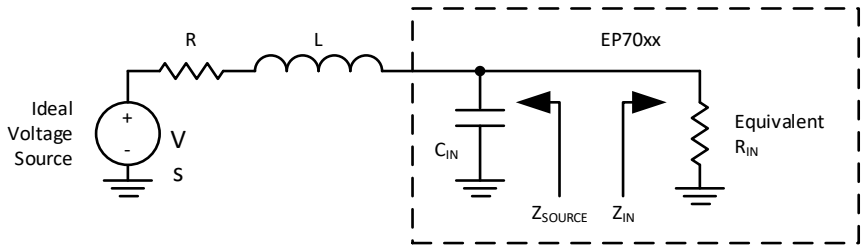

Figure 1. Input supply of EP71xx is modeled as an ideal voltage source, V_S, R and L of the PDN, and integrated input bypass capacitor C_{IN}

3. Steady State Input Voltage of EP71xx

The input source resistance, R, must be sufficiently small to maintain the input voltage within the EP71xx operating range of 2.97V to 3.63V over all load conditions and input voltage tolerance. The EP71xx supports up to 30W of output power which can require significant input current. The steady-state input voltage of the EP71xx, V_{IN}^{SS}, can be estimated as,

$$V_{IN}^{SS} = V_{S,min} - R \times \frac{P_{OUT,max}}{\eta \times V_{IN}^{SS}} \quad (1)$$

where $V_{S,min}$ is the minimum source voltage, R is the maximum source resistance, $P_{OUT,max}$ is the maximum power delivered to the load by the EP71xx, and η is the efficiency of the EP71xx at the maximum load current.

To ensure that V_{IN}^{SS} remains above the EP71xx minimum input voltage $V_{IN,min}^{SS} = 2.97V$ at all times,

$$R \leq \frac{\eta \times V_{IN,min}^{SS}}{P_{OUT,max}} \times \left(V_{S,min} - V_{IN,min}^{SS}\right) \quad (2)$$

Example:

Part number	EP7112
V_S	3.3V ± 5% (3.135V to 3.465V)
V_{OUT}	1V
$I_{OUT,max}$	12A
$P_{OUT,max}$	12W
η	80%

$$R \leq \frac{80\% \times 2.97V}{12W} \times (3.135V - 2.97V) = 32.6m\Omega$$

Under these conditions, the input source resistance must be less than 32.6mΩ to maintain the input voltage within the acceptable range of 2.97V to 3.63V.

4. Soft-Start and Dynamic Voltage Scaling (DVS)

Beyond the steady-state considerations for the input impedance, fast dynamic changes to the output voltage, such as soft-start or DVS, can cause the input voltage, V_{IN}, to drop or rise. Extra current is required of the EP71xx to charge the output capacitor, C_{OUT} (which is internal to the package of EP71xx) as well as any capacitive load C_{LOAD} (external to the EP71xx). The amount of current depends on the total output capacitance, $C_{OUT} + C_{LOAD}$, and the rate of change of the output voltage, $\frac{dV_{OUT}}{dt}$. With no additional capacitive load ($C_{LOAD} = 0$) and voltage rate of change less than 1mV/ns $\left(\frac{dV_{OUT}}{dt} < 1mV/ns\right)$ the effect on the input voltage is minimal, hence no additional input capacitance is needed.

The output capacitance for EP71xx family of products is approximately 2.68µF.

For a given output capacitance and capacitive load, the extra output current, $\Delta I_{OUT}^{dynamic}$, needed beyond the DC load during dynamic change of the output voltage is calculated as,

$$\Delta I_{OUT}^{dynamic} = \frac{dV_{OUT}}{dt} \times (C_{OUT} + C_{LOAD}) \quad (3)$$

And the extra input current required for dynamic voltage changes, $\Delta I_{IN}^{dynamic}$, can be calculated as,

$$\Delta I_{IN}^{dynamic} = \frac{V_{OUT}}{\eta \times V_{IN,min}} \times \frac{dV_{OUT}}{dt} \times (C_{OUT} + C_{LOAD}) \quad (4)$$

Therefore, the worst-case input voltage change, $\Delta V_{IN}^{dynamic}$, due solely to the dynamic output voltage change is,

$$\Delta V_{IN}^{dynamic} = -R \times \Delta I_{IN}^{dynamic} \quad (5)$$

Example:

Part number	EP7112
V_S	3.3V ± 5% (3.135V to 3.465V)
R	10 mΩ
V_{OUT}	1V
I_{OUT}	12A
$\frac{dV_{OUT}}{dt}$	1mV/ns
η	80%
C_{OUT}	2.68 µF
C_{LOAD}	0

$$V_{IN,min}^{SS} = 3.135V - 10\text{m}\Omega \times \frac{1V \times 12A}{80\% \times 3.135V} = 3.087V$$

$$V_{IN,min}^{dynamic} = V_{IN,min}^{SS} + \Delta V_{IN,max}^{dynamic} = 3.087\ V - \frac{10\ \text{m}\Omega\ \times\ 1.0\ V}{80\%\ \times\ V_{IN,min}^{dynamic}} \times\ 1\frac{mV}{ns} \times 2680nF$$

$$\left(V_{IN,min}^{dynamic}\right)^2 - \left(3.087\ V \times V_{IN,min}^{dynamic}\right) + \left(\frac{10\ \text{m}\Omega\ \times\ 1.0\ V}{80\%} \times 1\ \frac{mV}{ns} \times 2680nF\right) = 0$$

$$V_{IN,min}^{dynamic} \approx 3.076V$$

Over the above dynamic output voltage step conditions, the input voltage will drop down to 3.076V.

There may be cases where the input voltage drops below the minimum input voltage (i.e., 2.97V) due to dynamic output voltage changes. This can be remedied by adding input bypass capacitor C_{IN}. In this case, the input voltage drops mainly due to the energy lost from C_{IN} which is equal to the energy added to the output capacitor divided by the efficiency,

$$\Delta Q_{IN} = -\frac{V_{OUT} \times \Delta Q_{OUT}}{V_{IN} \times \eta}. \quad (6)$$

The voltage drop at C_{IN} can thus be calculated as,

$$V_{IN}^{dynamic} = \frac{\Delta Q_{IN}}{C_{IN}} = -\frac{V_{OUT} \times \Delta Q_{OUT}}{V_{IN} \times \eta \times C_{IN}} = \frac{V_{OUT} \times C_{OUT} \times \Delta V_{OUT}}{V_{IN} \times \eta \times C_{IN}} \quad (7)$$

Example:

Part number	EP7112
V_S	3.3V ± 5% (3.135V to 3.465V)
V_{OUT}	1.0V
ΔV_{OUT}	+400 mV
η	80%
C_{OUT}	2.68µF

$$V_{IN}^{dynamic} = V_{S,min} - V_{IN,min} = 3.135\ V - 2.97\ V = 165\ mV,$$

$$C_{IN} \geq \frac{V_{OUT} \times C_{OUT} \times \Delta V_{OUT}}{V_{IN} \times \eta \times V_{IN}^{dynamic}} = \frac{1V \times 2.68\ \mu F \times 400\ mV}{3.135\ V \times 80\% \times 165\ mV} \approx 2590\ \text{nF}$$

EP71xx device has input capacitance of 1340nF inside the package. Additional input capacitance of 1250nF must be added in this example to ensure the input voltage does not drop below the minimum voltage of 2.97V.

Table 1 through Table 2 tabulate the required additional minimum C_{IN} capacitor for various V_{OUT} and ΔV_{OUT} levels for EP7112 and each rail of EP7123. An 80% efficiency and 100 mV to 700mV variation in the output voltage, $V_{IN}^{dynamic} = 165mV$ and $V_{IN} = 3.135V$ is assumed in these calculations.

Table 1. Recommended minimum C_{IN} values for Dynamic Voltage Scaling (DVS) of EP7112

V_{OUT} [V]	**0.5**	**0.65**	**0.8**	**1.0**	**1.2**	**1.8**
ΔV_{OUT} [mV]	**Minimum C_{IN} [µF]**					
100	-	-	-	-	-	-
200	-	-	-	-	-	-
400	-	-	-	-	0.43	1.98
700	-	0.27	0.95	1.85	2.76	5.48

Table 2. Recommended minimum C_{IN} values for Dynamic Voltage Scaling (DVS) of EP7123 VR1/VR2

V_{OUT} [V]	0.5	0.65	0.8	1	1.2	1.8
ΔV_{OUT} [mV]	Minimum C_{IN} [µF]					
100	-	-	-	-	-	-
200	-	-	-	-	-	-
400	-	-	-	-	0.21	0.99
700	-	0.13	0.47	0.93	1.38	2.74

5. Negative Dynamic Input Resistance

Like any other switch-mode DC-DC voltage regulator, the EP71xx has a dynamic negative input resistance, because at a given output voltage, V_{OUT} and load current, I_{OUT}, the regulator output power is constant irrespective of fluctuations in the input voltage, V_{IN}. This creates a condition where, as the input voltage drops, the input current rises to maintain the constant output power, thus creating a negative dynamic input resistance. To ensure stability at the EP71xx input, the source impedance must be lower in magnitude than the EP71xx input negative resistance over the entire regulator loop bandwidth.

Over the entire EP71xx regulator control loop bandwidth, the simplified input dynamic impedance (for a fixed output voltage and load) is,

$$R_{INPUT} = \frac{\partial V_{IN}}{\partial I_{IN}} = -\frac{P_{OUT}/\eta}{{I_{IN}}^2} = -\frac{{V_{IN}}^2}{P_{OUT}/\eta} \quad (8)$$

And the minimum input dynamic resistance value is,

$$R_{INPUT,min} = -\frac{\eta \times {V_{IN,min}}^2}{P_{OUT,max}}, \quad (9)$$

where $P_{OUT,max}$ is the maximum EP71xx output power, and η is the power conversion efficiency.

Example:

Part number	EP7112
$V_{IN,min}$	2.97V
V_{OUT}	1V
$I_{OUT,max}$	12A
η	78.5%

$$R_{INPUT,min} = -\frac{78.5\% \times (2.97V)^2}{1V \times 12A} \approx -0.58\,\Omega$$

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6. System Stability

To ensure system stability with 6 dB gain margin, based on an extension to the Middlebrook Stability Criterion [1-2], select the input capacitor, C_{IN}, using the following,

$$|Z_O| < \frac{1}{2} \times |R_{INPUT,min}|, \tag{11}$$

where Z_O is the source power supply output impedance presented to the EP71xx input, including R, L and C_{IN}, as shown in Figure 2. Therefore, based on the previous example,

$$|Z_O| < \frac{1}{2} \times |R_{INPUT,min}| < 0.29\ \Omega \tag{12}$$

The following two examples show calculations to determine the input capacitance requirement for meeting the stability criterion.

Example 1: Large parasitic R and L *between* V_S *and* V_{IN} *(e.g.,* Empower EVMB/EVDT demo hardware)

R	10 mΩ
L	20 nH

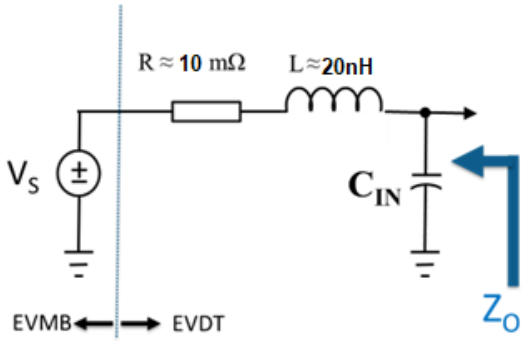

Figure 2. Equivalent input voltage source model with large voltage source parasitics

The small 30 mΩ resistance maintains the impedance below the EP71xx negative input impedance except around the parallel LC resonant frequency where the impedance peaks. The approximate maximum impedance at resonance is,

$$|Z_{O,max}| \approx \frac{L}{R \times C_{IN}},\ C_{IN} \geq \frac{L}{R \times |Z_{O,max}|} = \frac{20\ nH}{10\ m\Omega \times 0.29\ \Omega} \approx 6.90\mu F. \tag{13}$$

Given that EP71xx has $1.34\mu F$ of internal input capacitance, additional input capacitance of $5.56\mu F$ will be required for system stability.

Example 2: Small parasitic *R* and *L between* V_S *and* V_{IN}

R	3 mΩ
L	0.8 nH
ESR	10 mΩ

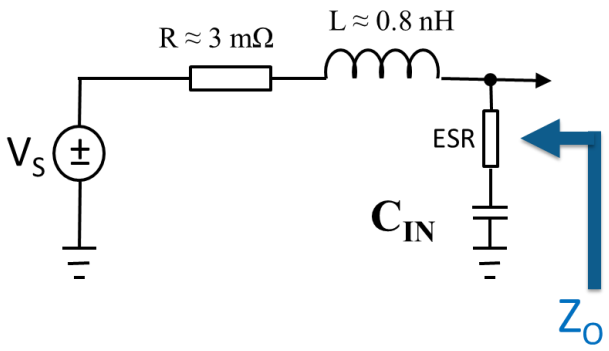

Figure 3. Equivalent input voltage source model with small PDN

Including the ESR of the input capacitor, the maximum input impedance is:

$$|Z_{O,max}| \approx \frac{L}{(R + ESR) \times C_{IN}}. \quad (14)$$

Therefore, for stability,

$$C_{IN} \geq \frac{L}{(R+ESR) \times |Z_{O,max}|} = \frac{0.8\ nH}{(3+10)\ m\Omega \times 0.29\ \Omega} \approx 210\ nF \quad (15)$$

Given that EP71xx has $1.34\ \mu F$ of internal input capacitance, there is sufficient input capacitance and no additional external capacitor will be required.

Table 3 tabulate the required additional minimum C_{IN} capacitor for various R and L values of the input PDN. The EP71xx features a configurable loop bandwidth setting. Contact Empower Semiconductor for more details.

Table 3. Recommended minimum C_{IN} values for system stability of EP71xx family products.

L [nH]	1	5	10	20	50
R[mΩ]	**Minimum C_{IN} [µF]**				
1	2.11	15.90	33.14	67.63	171.07
3	-	4.41	10.15	21.65	56.13
5	-	2.11	5.56	12.45	33.14
10	-	0.38	2.11	5.56	15.90
30	-	-	-	0.96	4.41
50	-	-	-	-	2.11

7. References

[1] R.D. Middlebrook, “Input filter consideration in design and application of switching regulators” in Proceedings of IEEE Industrial Applications Society Annual Meeting, 1976.

[2] Xiaogang Feng, Jinjun Liu, Fred C. Lee, “Impedance Specifications for Stable DC Distributed Power System” in IEEE Transactions on Power Electronics, Vol. 17 No. 2, March 2002.

8. Revision History

#	Date	Description	Version
1.	October 30, 2023	Initial version released.	1.0
2.	February 9th, 2024	Formatting Updates	1.1